2008-01-01

Unified Power Quality Conditioner: protection and performance enhancement

Iurie Axente
Technological University Dublin

5. Jayanti N. G., Malabika Basu, Iurie Axente, Kevin Gaughan and Michael F. Conlon, "Development of laboratory prototype of a 12KVA digital shunt active filter", *Proceedings of the 34th IEEE Industrial Electronics Society Conference (IECON), Florida,* USA, 10th –13th November 2008. (submitted)

List of publications

The research work reported in this thesis has resulted in the following papers:

1. Iurie Axente, Malabika Basu, Michael F. Conlon and Kevin Gaughan, "Protection of DVR against Short Circuit Faults at the Load Side", *Proceedings of the 3rd IEE International Conference on Power Electronics, Machines and Drives (PEMD) 2006*, Clontarf Castle, Dublin, Ireland, 4th – 6th April 2006.

2. Iurie Axente, Malabika Basu, Michael F. Conlon and Kevin Gaughan, "A Study of Shunt Active Filter Generating the DC Biased Current", *Proceedings of the 41st International Universities Power Engineering Conference (UPEC) 2006, Northumbria University, Newcastle upon Tyne*, UK, 6th –8th September 2006.

3. Iurie Axente, Malabika Basu, Michael F. Conlon, "A Control Approach for UPQC Connected to Week Supply Point", *Proceedings of the 42nd International Universities Power Engineering Conference (UPEC) 2007, University of Brighton, Brighton*, UK, 4th –6th September 2007.

4. Jayanti N. G., Malabika Basu, Iurie Axente, Kevin Gaughan and Michael F. Conlon, "Sequence analysis based DSP controller for Dynamic Voltage Restorer (DVR)", *Proceedings of the 39th IEEE Power Electronics Specialists Conference (PESC), Rhodes*, Greece, 15th –19th June 2008. (accepted)

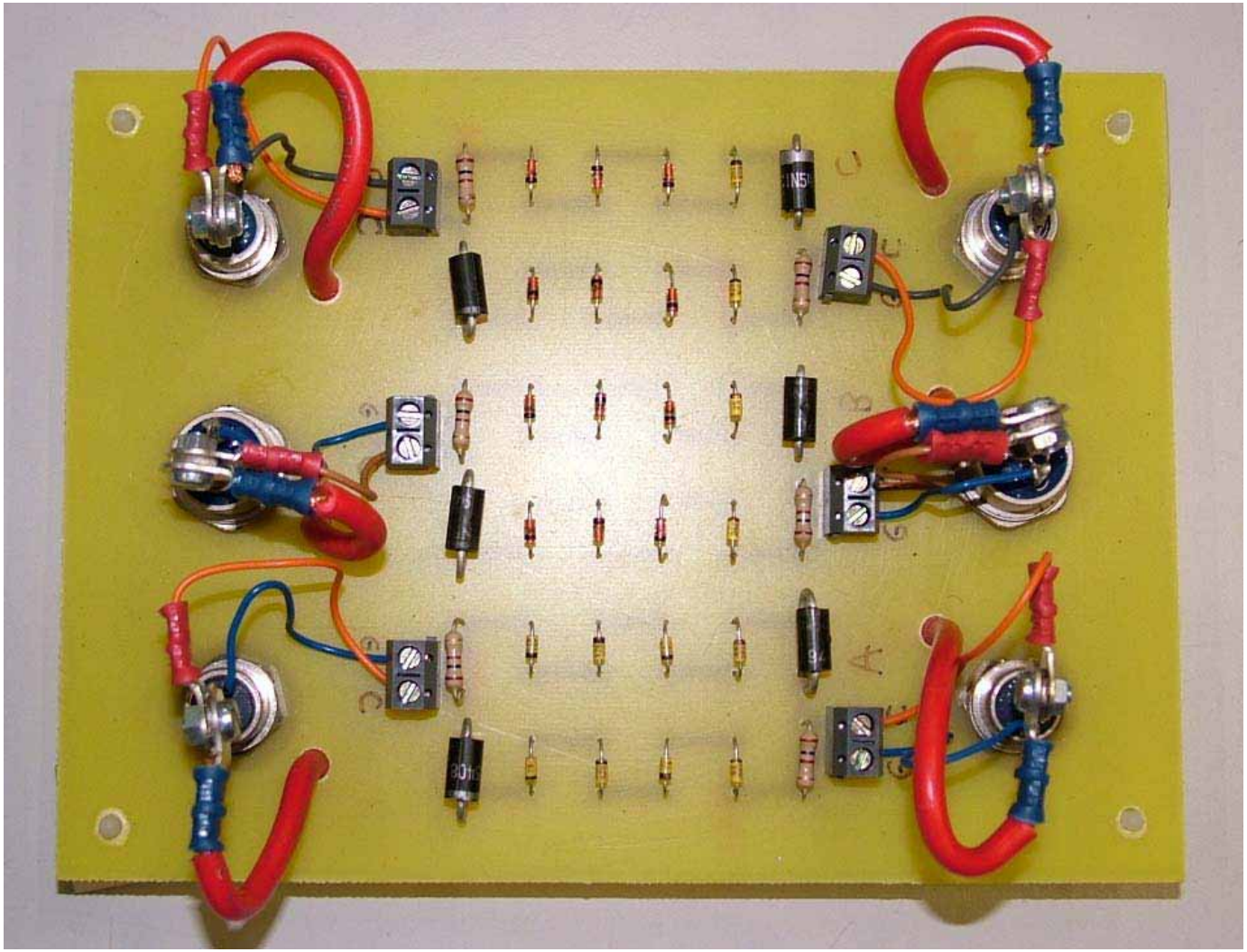


Fig.E3. Built circuit

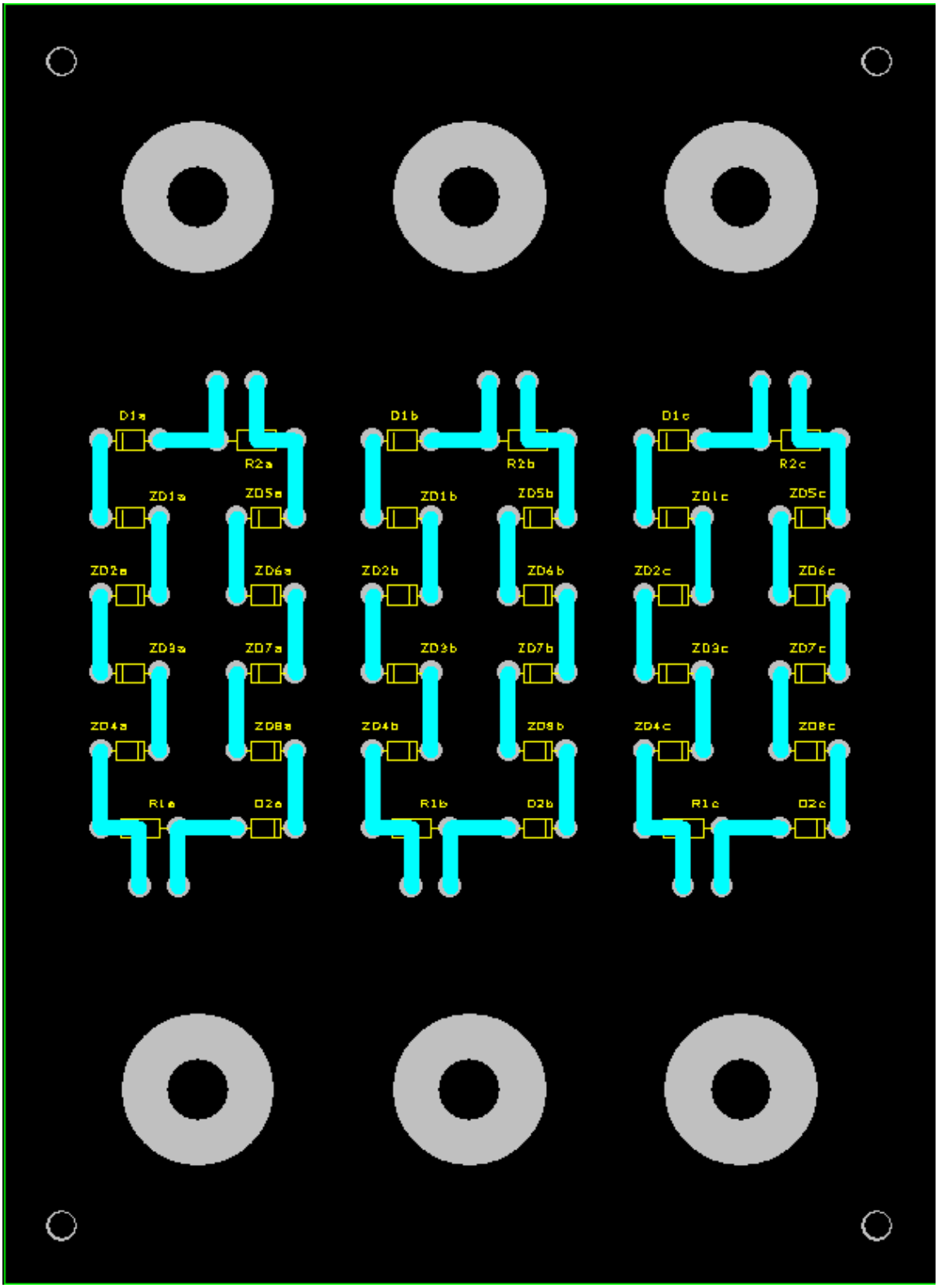


Fig.E2. PCB layout (designed with Easy-PC)

Appendix E. Protection crowbar

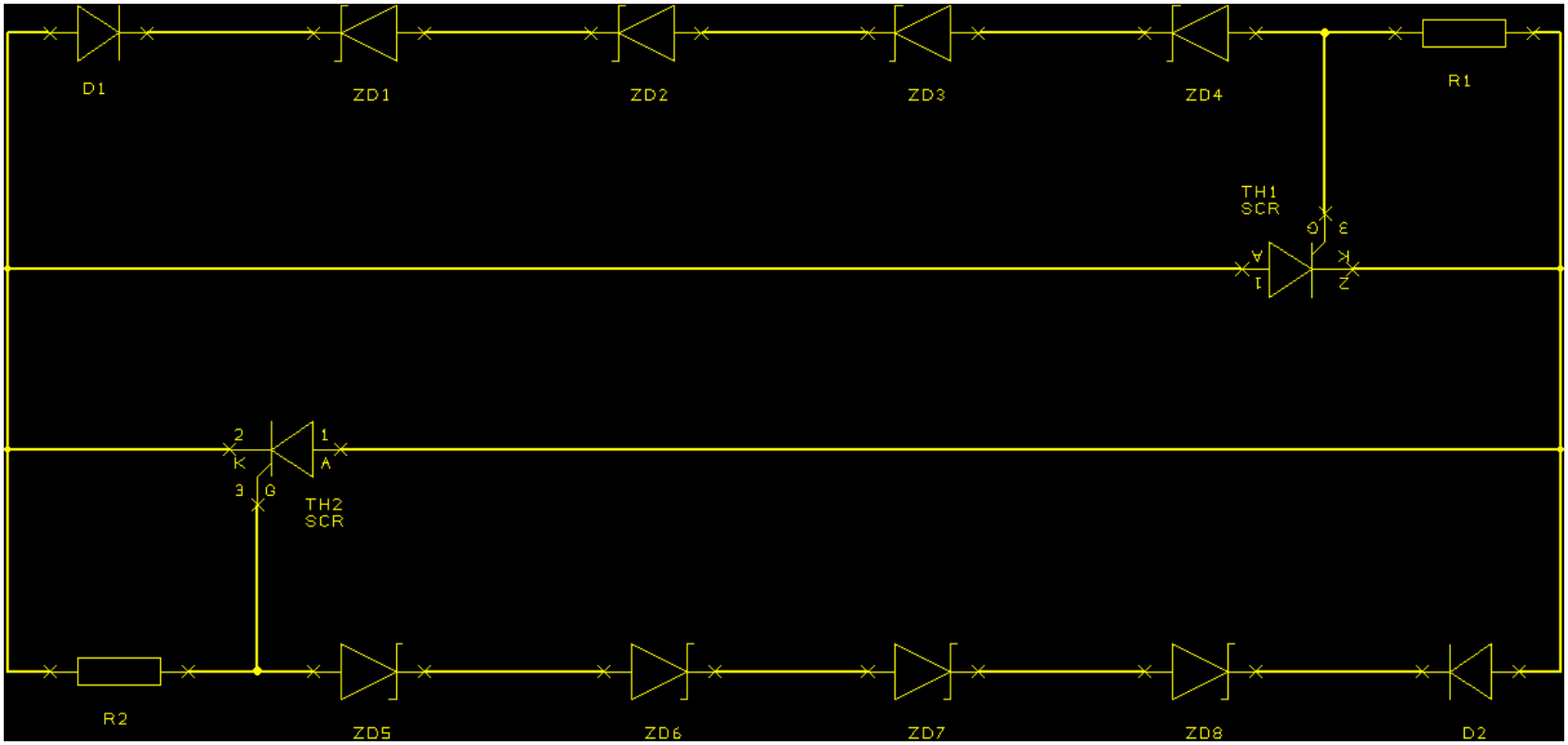
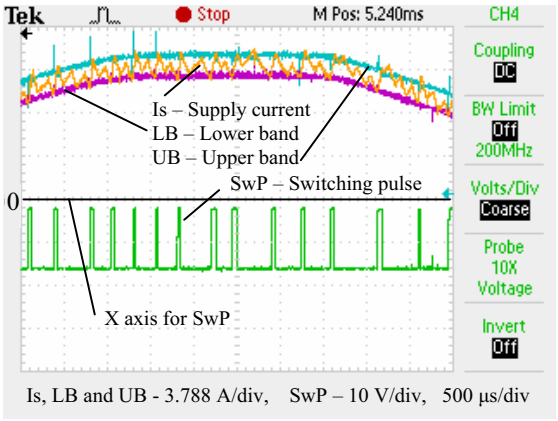
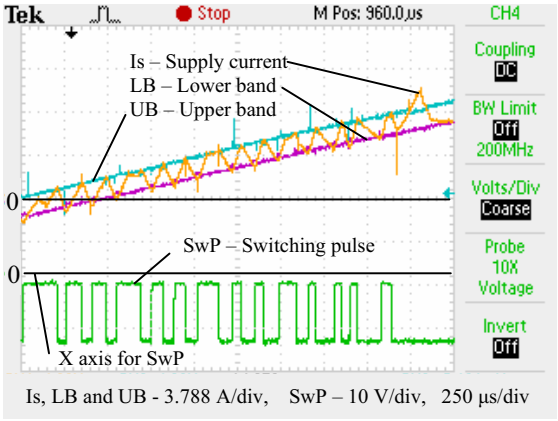


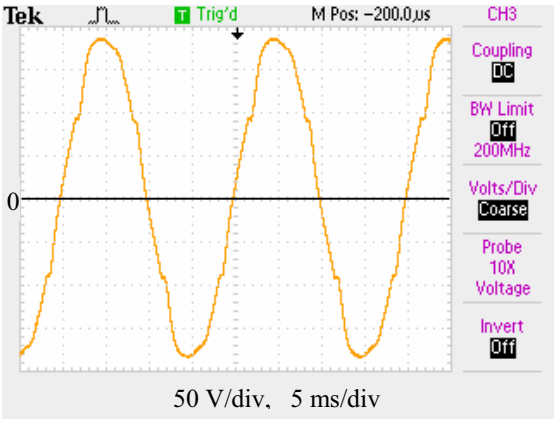
Fig.E1. Schematic layout for one phase (designed with Easy-PC)



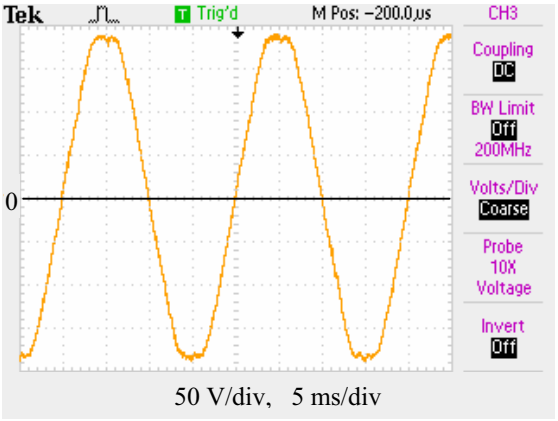
a) Hysteresis bands, supply current and switching pulses (portion 1)



b) Hysteresis bands, supply current and switching pulses (portion 2)

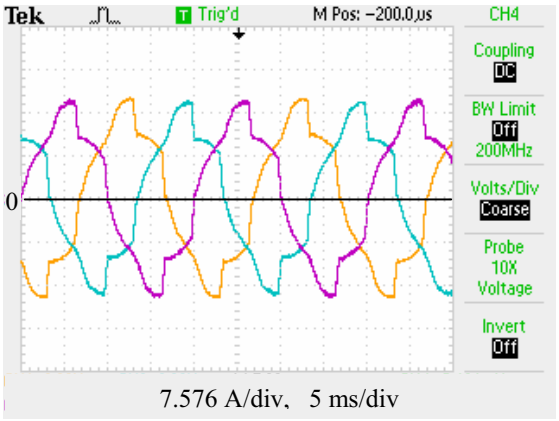


c) Supply voltage without compensation (THD=5.18%)

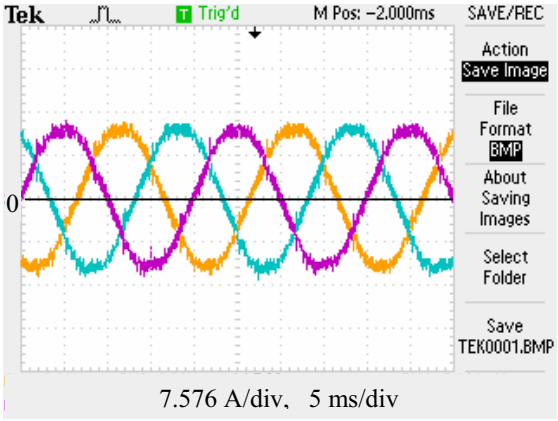


d) Supply voltage with compensation (THD=3.31%)

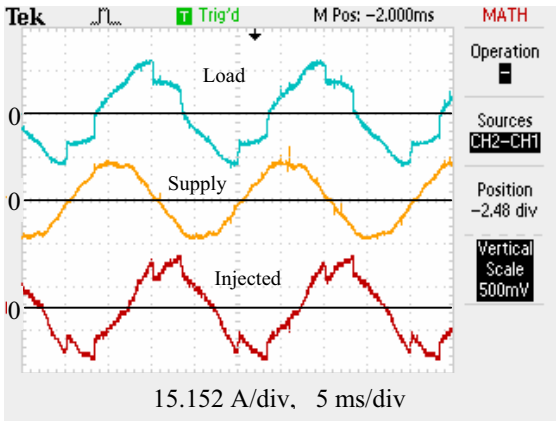
Fig.D5. Testing results (continuation)



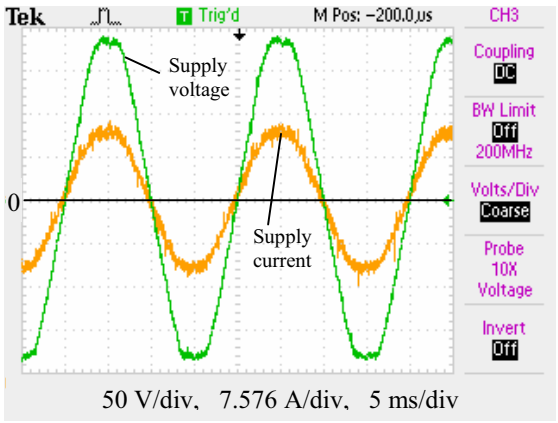
a) Load currents (THD=14.76%)



b) Supply currents (4.3%)



c) Load, supply and injected currents



d) Supply voltage and current

e) Hysteresis bands

f) Hysteresis bands and supply current

Fig.D4. Testing results

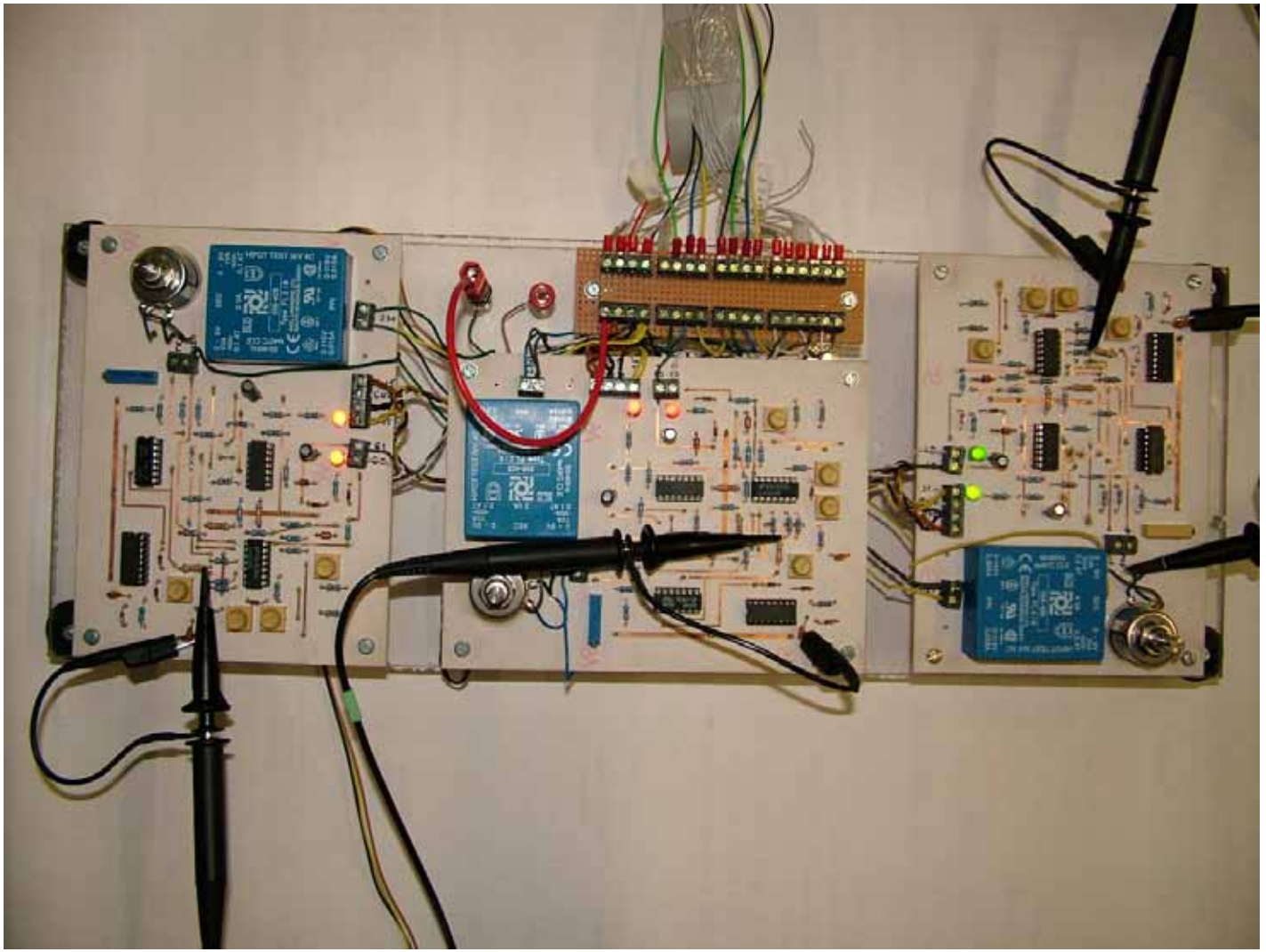


Fig.D3. Built controller in action

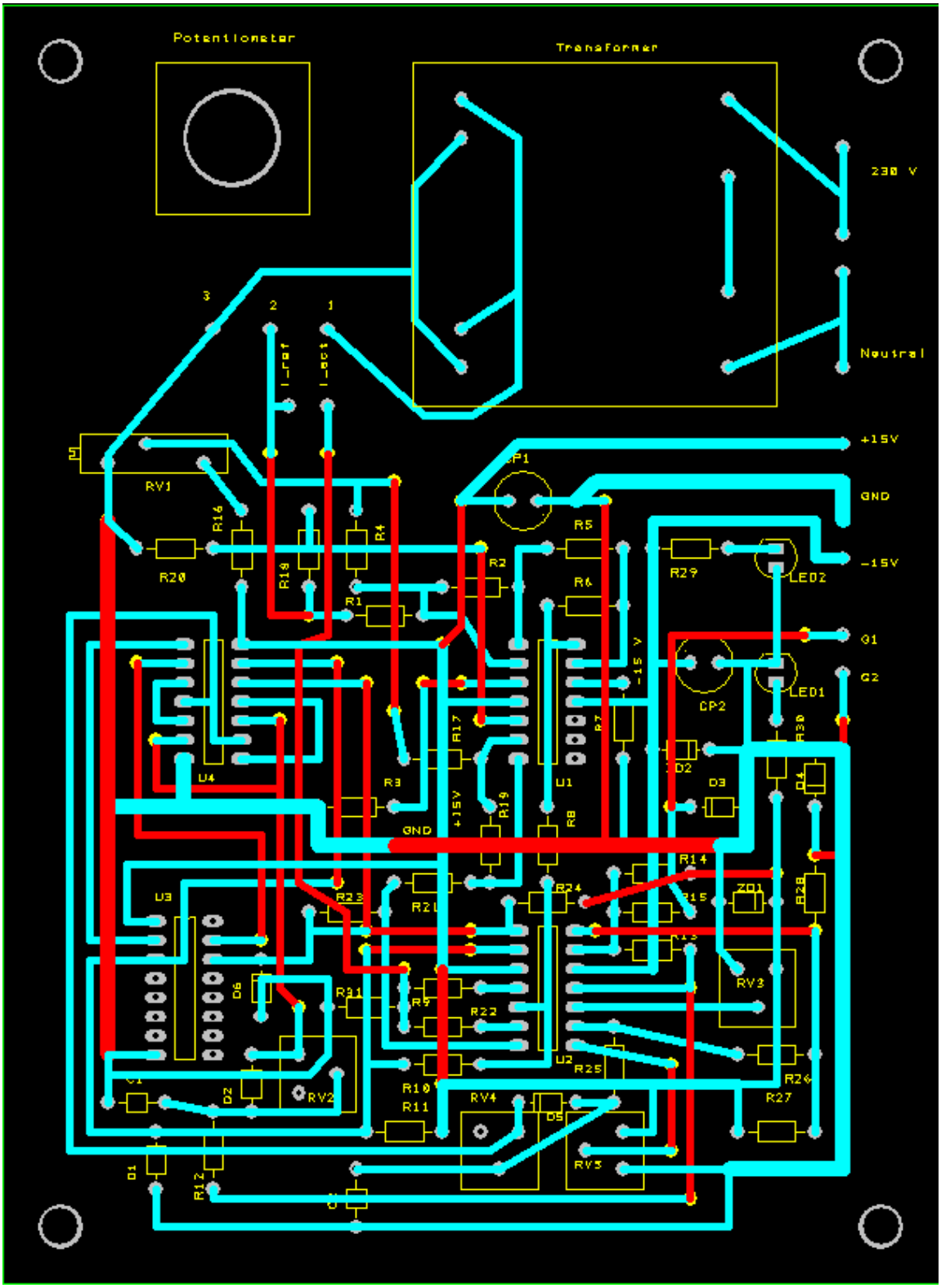


Fig.D2. PCB layout (designed with Easy-PC)

Appendix D. Analog hysteresis controller

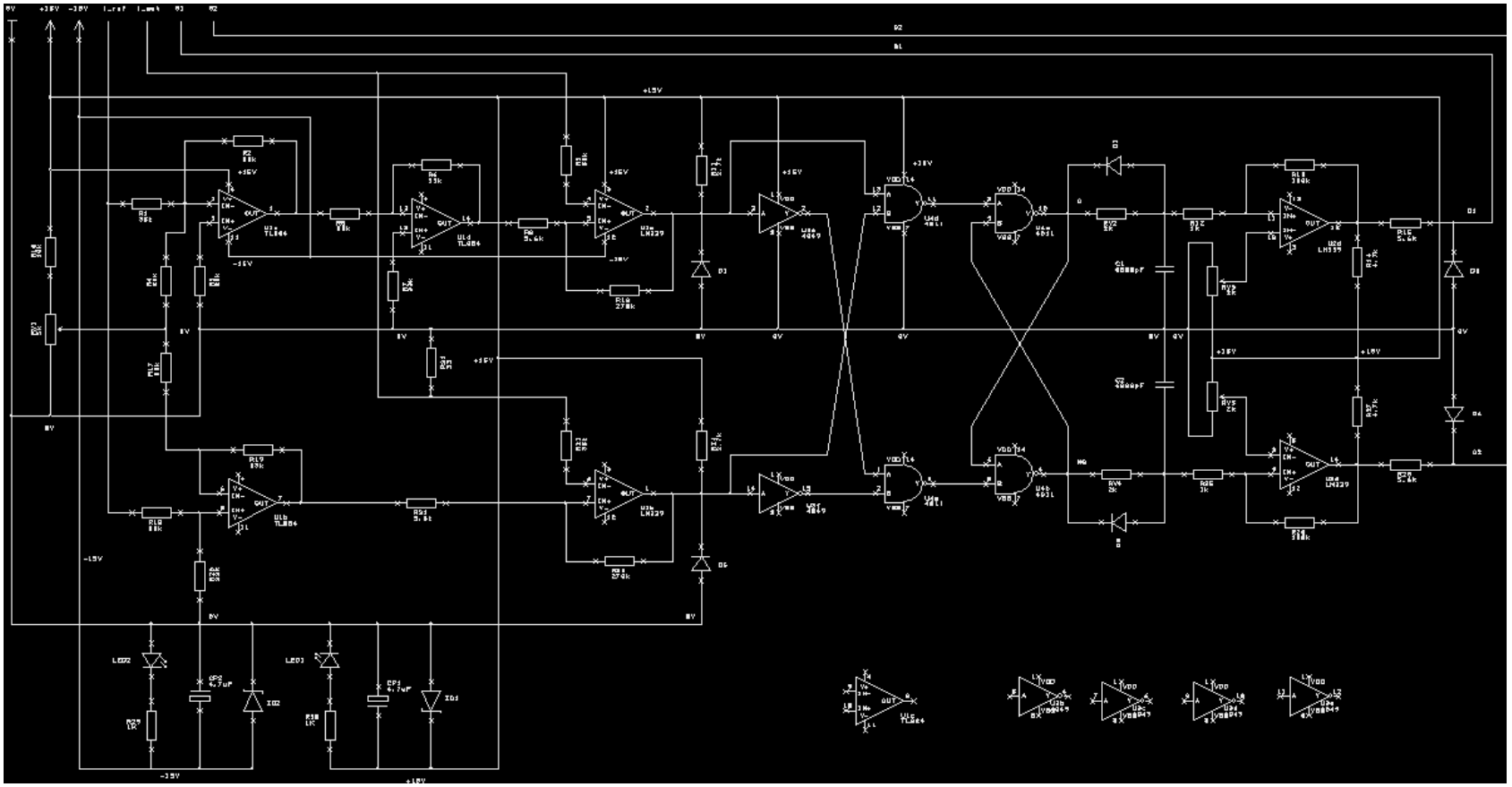


Fig.D1. Schematic layout (designed with Easy-PC)

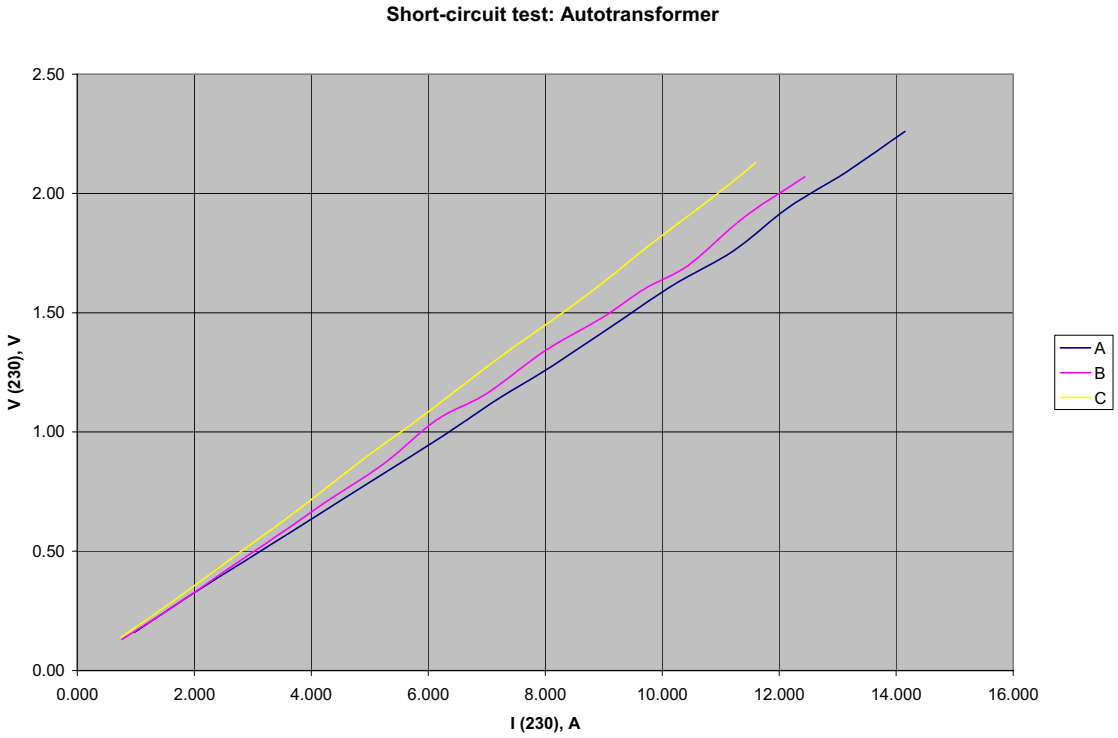


Fig.C4. Short-circuit characteristics of the shunt transformer

Table C11. Short-circuit test results and parameters of the shunt transformer, phase B

Short-circuit Test (phase B)													
I (230), A	V (230), V	P, W	I (130),A	Zeq (230), Ohm	Req (230), Ohm	Xeq (230), Ohm	Leq (230), mH	Req (130), Ohm	Xeq (130), Ohm	Leq (130), mH	Req, pu	Xeq, pu	Leq, pu
0.762	0.13	0.1	1.348	0.171	0.172		0.000	0.055	0.000	0.000	0.013	0.000	0.000
1.660	0.27	0.4	2.937	0.163	0.145	0.073	0.234	0.046	0.023	0.075	0.011	0.006	0.006
2.664	0.44	1.2	4.713	0.165	0.169		0.000	0.054	0.000	0.000	0.013	0.000	0.000
3.450	0.57	2.0	6.104	0.165	0.168		0.000	0.054	0.000	0.000	0.013	0.000	0.000
4.270	0.71	3.0	7.555	0.166	0.165	0.024	0.076	0.053	0.008	0.024	0.012	0.002	0.002
5.259	0.87	4.5	9.304	0.165	0.163	0.030	0.095	0.052	0.010	0.030	0.012	0.002	0.002
6.140	1.05	6.4	10.863	0.171	0.170	0.021	0.066	0.054	0.007	0.021	0.013	0.002	0.002
6.990	1.16	8.0	12.367	0.166	0.164	0.027	0.086	0.052	0.009	0.028	0.012	0.002	0.002
7.990	1.34	10.6	14.136	0.168	0.166	0.024	0.075	0.053	0.008	0.024	0.013	0.002	0.002
8.980	1.48	13.3	15.888	0.165	0.165		0.000	0.053	0.000	0.000	0.012	0.000	0.000
9.700	1.60	15.1	17.162	0.165	0.160	0.038	0.121	0.051	0.012	0.039	0.012	0.003	0.003
10.450	1.70	18.0	18.488	0.163	0.165		0.000	0.053	0.000	0.000	0.012	0.000	0.000
11.400	1.90	21.7	20.169	0.167	0.167		0.000	0.053	0.000	0.000	0.013	0.000	0.000
12.440	2.07	25.7	22.009	0.166	0.166	0.010	0.033	0.053	0.003	0.011	0.013	0.001	0.001
			Avearge:	0.166	0.165	0.031	0.056	0.053	0.006	0.018	0.012	0.001	0.001

Table C12. Short-circuit test results and parameters of the shunt transformer, phase C

Short-circuit Test (phase C)													
I (230), A	V (230), V	P, W	I (130),A	Zeq (230), Ohm	Req (230), Ohm	Xeq (230), Ohm	Leq (230), mH	Req (130), Ohm	Xeq (130), Ohm	Leq (130), mH	Req, pu	Xeq, pu	Leq, pu
0.750	0.14	0.1	1.327	0.187	0.178	0.057	0.181	0.057	0.018	0.058	0.013	0.004	0.004
1.575	0.28	0.4	2.787	0.178	0.161	0.075	0.238	0.052	0.024	0.076	0.012	0.006	0.006
2.472	0.44	1.0	4.374	0.178	0.164	0.070	0.223	0.052	0.022	0.071	0.012	0.005	0.005
3.195	0.57	1.8	5.653	0.178	0.176	0.027	0.086	0.056	0.009	0.028	0.013	0.002	0.002
3.970	0.71	2.7	7.024	0.179	0.171	0.051	0.163	0.055	0.016	0.052	0.013	0.004	0.004
4.800	0.87	4.0	8.492	0.181	0.174	0.052	0.166	0.055	0.017	0.053	0.013	0.004	0.004
5.700	1.03	5.6	10.085	0.181	0.172	0.054	0.173	0.055	0.017	0.055	0.013	0.004	0.004
6.400	1.16	7.1	11.323	0.181	0.173	0.053	0.169	0.055	0.017	0.054	0.013	0.004	0.004
7.310	1.33	9.4	12.933	0.182	0.176	0.046	0.148	0.056	0.015	0.047	0.013	0.004	0.004
8.183	1.48	11.7	14.478	0.181	0.175	0.047	0.149	0.056	0.015	0.047	0.013	0.004	0.004
8.950	1.62	14.2	15.835	0.181	0.177	0.037	0.116	0.057	0.012	0.037	0.013	0.003	0.003
9.870	1.80	17.2	17.462	0.182	0.177	0.046	0.145	0.056	0.015	0.046	0.013	0.003	0.003
10.740	1.96	20.4	19.002	0.182	0.177	0.045	0.143	0.057	0.014	0.046	0.013	0.003	0.003
11.600	2.13	23.6	20.523	0.184	0.175	0.054	0.173	0.056	0.017	0.055	0.013	0.004	0.004
			Avearge:	0.181	0.173	0.051	0.162	0.055	0.016	0.052	0.013	0.004	0.004

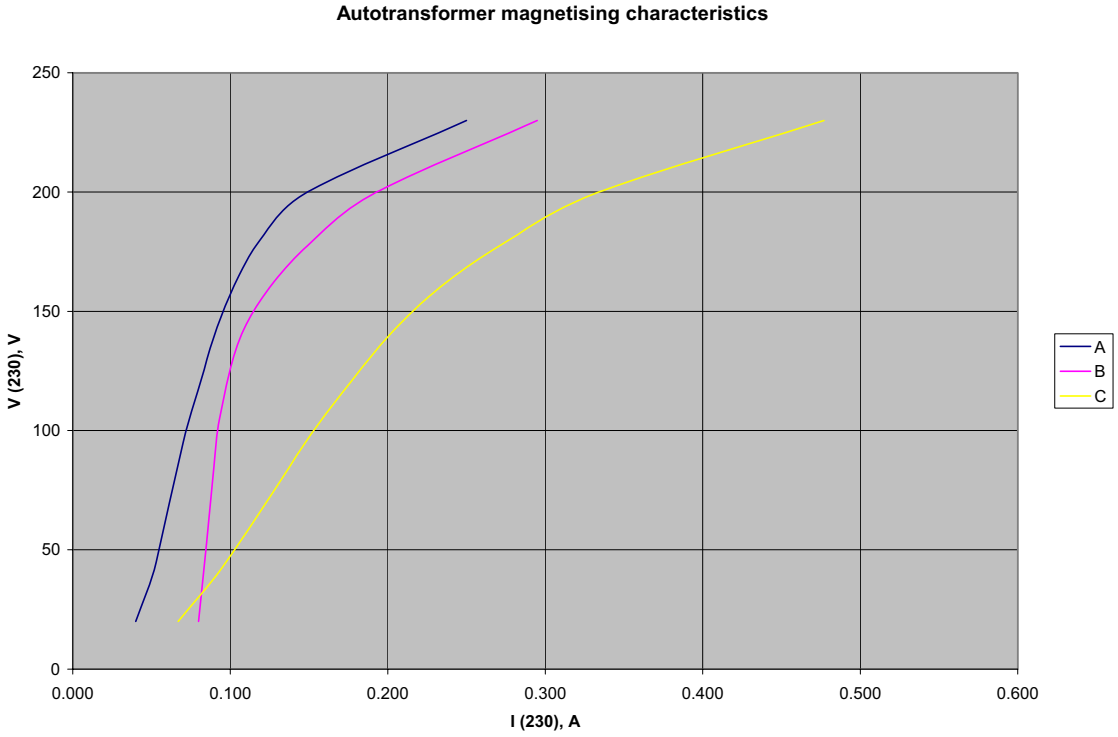


Fig.C3. Magnetising characteristics of the shunt transformer

Table C7. No-load test results and parameters of the shunt transformer, phase A

No-load Test (phase A)													
I (230), A	V (230), V	V (130), V	P, W	Tr. ratio	Rc (230), Ohm	Xm (230), Ohm	Lm (230), mH	Rc (130), Ohm	Xm (130), Ohm	Lm (130), mH	Rc, pu	Xm, pu	Lm, pu
0.040	20	11.12	0.3	1.799	1333.333	539.360	1716.836	425.961	172.310	548.479	100.819	40.783	40.783
0.051	40	22.24	1.3	1.799	1230.769	1017.726	3239.523	393.195	325.134	1034.933	93.064	76.955	76.955
0.058	60	33.3	2.8	1.802	1285.714	1742.081	5545.214	410.748	556.544	1771.534	97.218	131.726	131.726
0.065	80	44.4	4.7	1.802	1361.702	2876.586	9156.458	435.024	918.985	2925.220	102.964	217.511	217.511
0.072	100	55.5	6.9	1.802	1449.275	4862.166	15476.756	463.001	1553.320	4944.370	109.586	367.650	367.650
0.081	120	66.6	9.5	1.802	1515.789	7002.844	22290.745	484.250	2237.204	7121.240	114.615	529.516	529.516
0.090	140	77.8	12.3	1.799	1593.496	7171.265	22826.845	509.075	2291.009	7292.508	120.491	542.251	542.251
0.102	160	88.9	15.4	1.800	1662.338	4738.921	15084.454	531.068	1513.946	4819.041	125.697	358.331	358.331
0.119	180	100	18.6	1.800	1741.935	3049.874	9708.051	556.497	974.345	3101.438	131.715	230.614	230.614
0.149	200	111.1	22.1	1.800	1809.955	2000.926	6369.144	578.228	639.237	2034.755	136.859	151.299	151.299
0.250	230	127.8	26.5	1.800	1996.226	1036.657	3299.782	637.736	331.182	1054.184	150.943	78.386	78.386
			Avearge:	1.800	1543.685	3276.219	10428.528	493.162	1046.656	3331.609	116.725	247.729	247.729

Table C8. No-load test results and parameters of the shunt transformer, phase B

No-load Test (phase B)													
I (230), A	V (230), V	V (130), V	P, W	Tr. ratio	Rc (230), Ohm	Xm (230), Ohm	Lm (230), mH	Rc (130), Ohm	Xm (130), Ohm	Lm (130), mH	Rc, pu	Xm, pu	Lm, pu
0.080	20	11.12	0.0	1.799	400000.000	250.000	795.775	127788.280	79.868	254.227	30245.747	18.904	18.904
0.083	40	22.24	0.1	1.799	16000.000	482.146	1534.720	5111.531	154.032	490.298	1209.830	36.457	36.457
0.086	60	33.3	0.1	1.802	36000.000	697.805	2221.184	11500.945	222.928	709.603	2722.117	52.764	52.764
0.089	80	44.4	0.2	1.802	32000.000	899.231	2862.342	10223.062	287.278	914.434	2419.660	67.995	67.995
0.092	100	55.5	0.7	1.802	14285.714	1090.117	3469.949	4563.867	348.260	1108.547	1080.205	82.428	82.428
0.098	120	66.6	1.4	1.802	10285.714	1233.260	3925.589	3285.984	393.990	1254.111	777.748	93.252	93.252
0.107	140	77.8	2.2	1.799	8909.091	1322.754	4210.457	2846.194	422.581	1345.117	673.655	100.019	100.019
0.125	160	88.9	3.4	1.800	7529.412	1298.907	4134.549	2405.426	414.963	1320.867	569.332	98.216	98.216
0.153	180	100	4.4	1.800	7363.636	1191.779	3793.552	2352.466	380.739	1211.929	556.797	90.116	90.116
0.193	200	111.1	5.6	1.800	7142.857	1047.350	3333.819	2281.934	334.598	1065.057	540.103	79.195	79.195
0.295	230	127.8	8.2	1.800	6451.220	785.418	2500.063	2060.976	250.918	798.697	487.805	59.389	59.389
			Avearge:	1.800	49633.422	936.252	2980.182	15856.424	299.105	952.081	3753.000	70.794	70.794

Table C9. No-load test results and parameters of the shunt transformer, phase C

No-load Test (phase C)													
I (230), A	V (230), V	V (130), V	P, W	Tr. ratio	Rc (230), Ohm	Xm (230), Ohm	Lm (230), mH	Rc (130), Ohm	Xm (130), Ohm	Lm (130), mH	Rc, pu	Xm, pu	Lm, pu
0.067	20	11.12	0.7	1.799	571.429	350.070	1114.307	182.555	111.837	355.989	43.208	26.470	26.470
0.092	40	22.24	2.5	1.799	640.000	592.495	1885.970	204.461	189.285	602.512	48.393	44.801	44.801
0.113	60	33.3	5.1	1.802	705.882	805.823	2565.014	225.509	257.437	819.447	53.375	60.932	60.932
0.133	80	44.4	8.4	1.802	761.905	979.992	3119.411	243.406	313.079	996.560	57.611	74.101	74.101
0.153	100	55.5	12.3	1.802	813.008	1098.967	3498.122	259.732	351.088	1117.547	61.475	83.098	83.098
0.176	120	66.6	17.1	1.802	842.105	1161.727	3697.892	269.028	371.138	1181.368	63.675	87.843	87.843
0.201	140	77.8	22.7	1.799	863.436	1178.566	3751.492	275.843	376.517	1198.492	65.288	89.117	89.117
0.233	160	88.9	29.2	1.800	876.712	1104.559	3515.919	280.084	352.874	1123.233	66.292	83.521	83.521
0.277	180	100	36.8	1.800	880.435	963.084	3065.591	281.273	307.677	979.366	66.574	72.823	72.823
0.334	200	111.1	46.0	1.800	869.565	825.798	2628.596	277.801	263.818	839.760	65.752	62.442	62.442
0.477	230	127.8	64.3	1.800	822.706	595.104	1894.275	262.830	190.118	605.165	62.208	44.998	44.998
			Avearge:	1.800	786.108	877.835	2794.235	251.138	280.443	892.676	59.441	66.377	66.377

Table C10. Short-circuit test results and parameters of the shunt transformer, phase A

Short-circuit Test (phase A)													
I (230), A	V (230), V	P, W	I (130),A	Zeq (230), Ohm	Req (230), Ohm	Xeq (230), Ohm	Leq (230), mH	Req (130), Ohm	Xeq (130), Ohm	Leq (130), mH	Req, pu	Xeq, pu	Leq, pu
0.974	0.16	0.1	1.723	0.164	0.105	0.126	0.401	0.034	0.040	0.128	0.008	0.010	0.010
2.026	0.33	0.6	3.584	0.163	0.146	0.072	0.229	0.047	0.023	0.073	0.011	0.005	0.005
3.195	0.51	1.6	5.653	0.160	0.157	0.030	0.096	0.050	0.010	0.031	0.012	0.002	0.002
4.100	0.65	2.6	7.254	0.159	0.155	0.035	0.111	0.049	0.011	0.035	0.012	0.003	0.003
5.064	0.80	4.0	8.959	0.158	0.156	0.025	0.080	0.050	0.008	0.025	0.012	0.002	0.002
6.100	0.96	5.8	10.792	0.157	0.156	0.022	0.069	0.050	0.007	0.022	0.012	0.002	0.002
7.200	1.14	8.0	12.738	0.158	0.154	0.035	0.113	0.049	0.011	0.036	0.012	0.003	0.003
8.010	1.26	9.8	14.172	0.157	0.153	0.038	0.120	0.049	0.012	0.038	0.012	0.003	0.003
9.060	1.43	12.7	16.029	0.158	0.155	0.031	0.099	0.049	0.010	0.032	0.012	0.002	0.002
10.150	1.61	16.0	17.958	0.159	0.155	0.032	0.103	0.050	0.010	0.033	0.012	0.002	0.002
11.220	1.76	19.3	19.851	0.157	0.153	0.033	0.106	0.049	0.011	0.034	0.012	0.003	0.003
12.150	1.94	23.1	21.496	0.160	0.156	0.032	0.101	0.050	0.010	0.032	0.012	0.002	0.002
13.150	2.09	27.0	23.265	0.159	0.156	0.030	0.094	0.050	0.009	0.030	0.012	0.002	0.002
14.150	2.26	31.3	25.035	0.160	0.156	0.033	0.104	0.050	0.010	0.033	0.012	0.002	0.002
			Avearge:	0.159	0.151	0.041	0.130	0.048	0.013	0.042	0.011	0.003	0.003

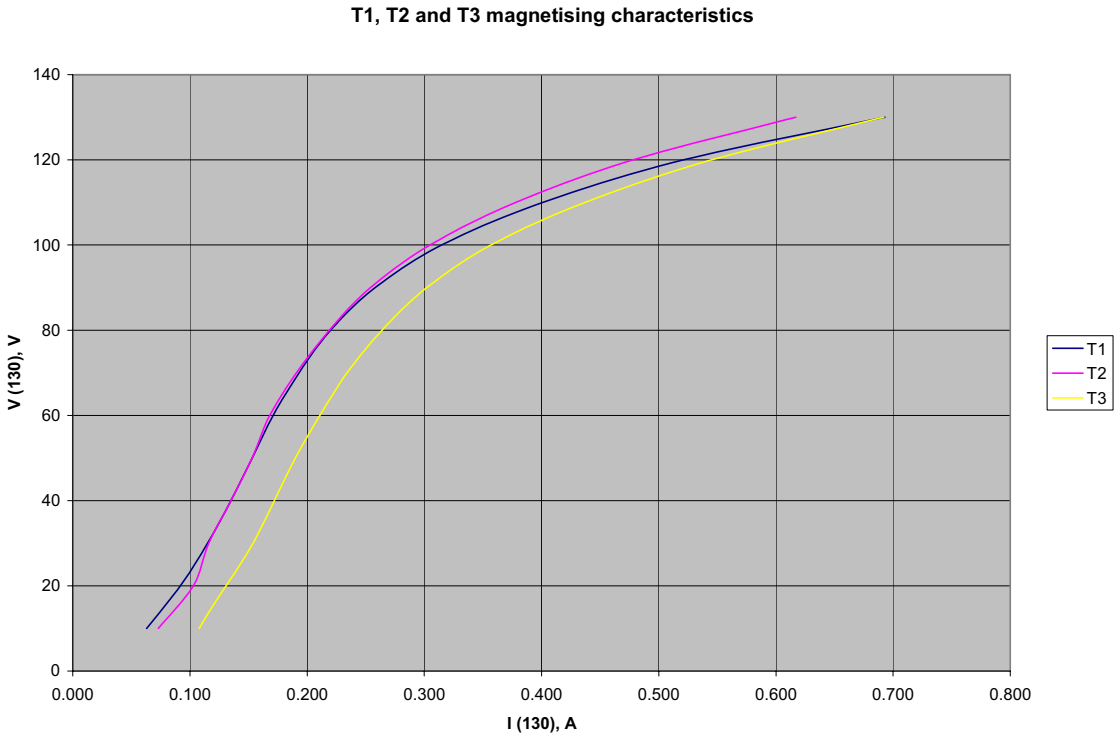


Fig.C1. Magnetising characteristics of the series transformers

Fig.C2. Short-circuit characteristics of the series transformers

Table C5. Short-circuit test results and parameters of the series transformer T2

Short-circuit Test (T2)													
I (130), A	V (130), V	P, W	I (115),A	Zeq (130), Ohm	Req (130), Ohm	Xeq (130), Ohm	Leq (130), mH	Req (115), Ohm	Xeq (115), Ohm	Leq (115), mH	Req, pu	Xeq, pu	Leq, pu
0.977	0.22	0.2	1.104	0.225	0.210	0.082	0.263	0.164	0.065	0.205	0.050	0.020	0.020
2.128	0.47	0.7	2.406	0.221	0.155	0.158	0.502	0.121	0.123	0.393	0.037	0.037	0.037
3.032	0.67	1.5	3.427	0.221	0.163	0.149	0.474	0.128	0.117	0.371	0.039	0.035	0.035
4.007	0.88	2.5	4.530	0.220	0.156	0.155	0.493	0.122	0.121	0.386	0.037	0.037	0.037
5.059	1.11	4.0	5.719	0.219	0.156	0.154	0.490	0.122	0.121	0.384	0.037	0.036	0.036
6.178	1.36	6.0	6.984	0.220	0.157	0.154	0.491	0.123	0.121	0.384	0.037	0.036	0.036
6.933	1.52	7.6	7.837	0.219	0.158	0.152	0.483	0.124	0.119	0.378	0.037	0.036	0.036
8.105	1.78	10.4	9.162	0.220	0.158	0.152	0.484	0.124	0.119	0.379	0.037	0.036	0.036
9.262	2.03	13.5	10.470	0.219	0.157	0.153	0.486	0.123	0.119	0.380	0.037	0.036	0.036
10.053	2.21	15.9	11.364	0.220	0.157	0.154	0.489	0.123	0.120	0.382	0.037	0.036	0.036
11.210	2.46	19.8	12.672	0.219	0.158	0.153	0.486	0.123	0.120	0.380	0.037	0.036	0.036
12.017	2.64	22.8	13.584	0.220	0.158	0.153	0.486	0.124	0.120	0.381	0.037	0.036	0.036
13.256	2.91	27.7	14.985	0.220	0.158	0.153	0.486	0.123	0.120	0.381	0.037	0.036	0.036
14.085	3.09	31.3	15.922	0.219	0.158	0.152	0.485	0.123	0.119	0.380	0.037	0.036	0.036
15.291	3.36	37.0	17.285	0.220	0.158	0.152	0.485	0.124	0.119	0.380	0.037	0.036	0.036
16.101	3.53	41.0	18.201	0.219	0.158	0.152	0.483	0.124	0.119	0.378	0.037	0.036	0.036
17.277	3.80	47.2	19.531	0.220	0.158	0.153	0.487	0.124	0.120	0.381	0.037	0.036	0.036
18.100	3.98	51.9	20.461	0.220	0.158	0.152	0.485	0.124	0.119	0.380	0.037	0.036	0.036
19.030	4.21	58.0	21.512	0.221	0.160	0.153	0.486	0.125	0.119	0.380	0.038	0.036	0.036
20.166	4.43	64.3	22.796	0.220	0.158	0.153	0.485	0.124	0.119	0.380	0.037	0.036	0.036
21.250	4.67	71.6	24.022	0.220	0.159	0.152	0.484	0.124	0.119	0.379	0.038	0.036	0.036
22.270	4.90	78.8	25.175	0.220	0.159	0.152	0.484	0.124	0.119	0.379	0.038	0.036	0.036
23.230	5.11	85.6	26.260	0.220	0.159	0.152	0.485	0.124	0.119	0.380	0.038	0.036	0.036
24.200	5.33	93.3	27.357	0.220	0.159	0.152	0.484	0.125	0.119	0.379	0.038	0.036	0.036
25.160	5.54	100.8	28.442	0.220	0.159	0.152	0.484	0.125	0.119	0.379	0.038	0.036	0.036
26.100	5.76	108.5	29.504	0.221	0.159	0.153	0.486	0.125	0.120	0.381	0.038	0.036	0.036
27.000	5.96	116.4	30.522	0.221	0.160	0.152	0.485	0.125	0.119	0.380	0.038	0.036	0.036
			Avearge:	0.220	0.160	0.150	0.478	0.125	0.117	0.374	0.038	0.036	0.036

Table C6. Short-circuit test results and parameters of the series transformer T3

Short-circuit Test (T3)													
I (130), A	V (130), V	P, W	I (115),A	Zeq (130), Ohm	Req (130), Ohm	Xeq (130), Ohm	Leq (130), mH	Req (115), Ohm	Xeq (115), Ohm	Leq (115), mH	Req, pu	Xeq, pu	Leq, pu
1.150	0.30	0.3	1.300	0.261	0.227	0.129	0.410	0.178	0.101	0.321	0.054	0.030	0.030
2.020	0.53	0.8	2.283	0.262	0.196	0.174	0.555	0.153	0.136	0.434	0.046	0.041	0.041
3.143	0.82	1.9	3.553	0.261	0.192	0.176	0.561	0.151	0.138	0.439	0.046	0.042	0.042
4.133	1.08	3.2	4.672	0.261	0.187	0.182	0.580	0.147	0.143	0.454	0.044	0.043	0.043
5.226	1.37	5.2	5.908	0.262	0.190	0.180	0.574	0.149	0.141	0.449	0.045	0.043	0.043
6.085	1.59	7.0	6.879	0.261	0.189	0.180	0.574	0.148	0.141	0.449	0.045	0.043	0.043
7.223	1.89	9.8	8.165	0.262	0.188	0.182	0.580	0.147	0.143	0.454	0.044	0.043	0.043
8.090	2.12	12.3	9.145	0.262	0.188	0.183	0.581	0.147	0.143	0.455	0.044	0.043	0.043
9.270	2.43	16.2	10.479	0.262	0.189	0.182	0.580	0.148	0.143	0.454	0.045	0.043	0.043
10.197	2.67	19.6	11.527	0.262	0.188	0.182	0.578	0.148	0.142	0.453	0.045	0.043	0.043
11.090	2.91	23.2	12.537	0.262	0.189	0.182	0.581	0.148	0.143	0.454	0.045	0.043	0.043
12.284	3.22	28.5	13.886	0.262	0.189	0.182	0.579	0.148	0.142	0.453	0.045	0.043	0.043
13.200	3.46	33.0	14.922	0.262	0.189	0.181	0.577	0.148	0.142	0.451	0.045	0.043	0.043
14.220	3.73	38.3	16.075	0.262	0.189	0.181	0.578	0.148	0.142	0.452	0.045	0.043	0.043
15.280	4.01	44.2	17.273	0.262	0.189	0.182	0.579	0.148	0.142	0.453	0.045	0.043	0.043
16.000	4.20	48.5	18.087	0.263	0.189	0.182	0.578	0.148	0.142	0.453	0.045	0.043	0.043
17.070	4.48	55.2	19.297	0.262	0.189	0.182	0.578	0.148	0.142	0.452	0.045	0.043	0.043
18.070	4.74	61.9	20.427	0.262	0.190	0.181	0.577	0.148	0.142	0.452	0.045	0.043	0.043
19.000	4.99	68.5	21.478	0.263	0.190	0.182	0.578	0.148	0.142	0.452	0.045	0.043	0.043
20.250	5.31	78.0	22.891	0.262	0.190	0.180	0.575	0.149	0.141	0.450	0.045	0.043	0.043
21.500	5.68	88.6	24.304	0.264	0.192	0.182	0.579	0.150	0.142	0.453	0.045	0.043	0.043
22.130	5.82	93.5	25.017	0.263	0.191	0.181	0.576	0.149	0.142	0.451	0.045	0.043	0.043
23.040	6.07	101.5	26.045	0.263	0.191	0.181	0.577	0.150	0.142	0.451	0.045	0.043	0.043
24.210	6.38	112.2	27.368	0.264	0.191	0.181	0.577	0.150	0.142	0.451	0.045	0.043	0.043
25.230	6.67	122.2	28.521	0.264	0.192	0.182	0.579	0.150	0.142	0.453	0.045	0.043	0.043
26.100	6.9	131	29.504	0.264	0.192	0.181	0.577	0.150	0.142	0.452	0.046	0.043	0.043
27.200	7.2	142.5	30.748	0.265	0.193	0.182	0.578	0.151	0.142	0.452	0.046	0.043	0.043
28.110	7.45	152.6	31.777	0.265	0.193	0.182	0.578	0.151	0.142	0.452	0.046	0.043	0.043
29.250	7.77	165.7	33.065	0.266	0.194	0.182	0.579	0.152	0.142	0.453	0.046	0.043	0.043
			Avearge:	0.263	0.190	0.181	0.577	0.149	0.142	0.452	0.045	0.043	0.043

Appendix C. Transformers test results

Table C1. No-load test results and parameters of the series transformer T1

No-load Test (T1)													
I (130), A	V (130), V	V (115), V	P, W	Tr. ratio	Rc (130), Ohm	Xm (130), Ohm	Lm (130), mH	Rc (115), Ohm	Xm (115), Ohm	Lm (115), mH	Rc, pu	Xm, pu	Lm, pu
0.063	10	9	0.3	1.111	333.333	180.510	574.582	260.848	141.257	449.636	78.895	42.724	42.724
0.092	20	17	1.1	1.176	363.636	271.188	863.218	284.562	212.217	675.507	86.068	64.187	64.187
0.115	30	26	2.3	1.154	391.304	349.993	1114.063	306.213	273.885	871.804	92.616	82.839	82.839
0.135	40	35	3.8	1.143	421.053	417.029	1327.444	329.492	326.344	1038.784	99.657	98.705	98.705
0.153	50	44	5.6	1.136	446.429	479.684	1526.881	349.350	375.374	1194.852	105.664	113.535	113.535
0.171	60	53	7.7	1.132	467.532	530.920	1689.972	365.865	415.469	1322.478	110.659	125.662	125.662
0.193	70	62	10.0	1.129	490.000	539.407	1716.984	383.447	422.110	1343.616	115.976	127.670	127.670
0.220	80	71	12.7	1.127	503.937	525.243	1671.902	394.353	411.026	1308.337	119.275	124.318	124.318
0.258	90	80	15.7	1.125	515.924	473.467	1507.092	403.733	370.509	1179.366	122.112	112.063	112.063
0.315	100	89	18.9	1.124	529.101	396.825	1263.134	414.045	310.533	988.459	125.231	93.923	93.923
0.401	110	98	22.6	1.122	535.398	319.426	1016.763	418.973	249.965	795.662	126.721	75.604	75.604
0.521	120	107	26.8	1.121	537.313	254.937	811.489	420.472	199.499	635.026	127.175	60.340	60.340
0.693	130	116	31.6	1.121	534.810	200.317	637.630	418.513	156.757	498.974	126.582	47.412	47.412
			Avearge:	1.132	466.905	379.919	1209.320	365.374	297.303	946.346	110.510	89.922	89.922

Table C2. No-load test results and parameters of the series transformer T2

No-load Test (T2)													
I (130), A	V (130), V	V (115), V	P, W	Tr. ratio	Rc (130), Ohm	Xm (130), Ohm	Lm (130), mH	Rc (115), Ohm	Xm (115), Ohm	Lm (115), mH	Rc, pu	Xm, pu	Lm, pu
0.073	10	9	0.3	1.111	333.333	150.261	478.297	260.848	117.586	374.288	78.895	35.565	35.565
0.103	20	17	1.1	1.176	363.636	229.658	731.023	284.562	179.717	572.058	86.068	54.357	54.357
0.116	30	26	2.3	1.154	391.304	344.618	1096.952	306.213	269.679	858.414	92.616	81.566	81.566
0.135	40	35	3.8	1.143	421.053	417.029	1327.444	329.492	326.344	1038.784	99.657	98.705	98.705
0.153	50	44	5.6	1.136	446.429	479.684	1526.881	349.350	375.374	1194.852	105.664	113.535	113.535
0.168	60	53	7.7	1.132	467.532	553.411	1761.563	365.865	433.069	1378.501	110.659	130.985	130.985
0.191	70	62	10.0	1.129	490.000	552.143	1757.527	383.447	432.077	1375.343	115.976	130.685	130.685
0.219	80	71	12.7	1.127	503.937	530.285	1687.949	394.353	414.971	1320.895	119.275	125.511	125.511
0.254	90	80	15.7	1.125	515.924	487.484	1551.708	403.733	381.478	1214.281	122.112	115.381	115.381
0.305	100	89	19.0	1.124	526.316	419.130	1334.131	411.865	327.988	1044.017	124.572	99.202	99.202
0.378	110	98	22.5	1.122	537.778	346.047	1101.501	420.835	270.797	861.974	127.285	81.905	81.905
0.478	120	107	26.7	1.121	539.326	283.649	902.884	422.046	221.968	706.547	127.651	67.136	67.136
0.617	130	116	31.4	1.121	538.217	228.971	728.838	421.178	179.180	570.348	127.389	54.194	54.194
			Avearge:	1.132	467.291	386.336	1229.746	365.676	302.325	962.331	110.601	91.441	91.441

Table C3. No-load test results and parameters of the series transformer T3

No-load Test (T3)													
I (130), A	V (130), V	V (115), V	P, W	Tr. ratio	Rc (130), Ohm	Xm (130), Ohm	Lm (130), mH	Rc (115), Ohm	Xm (115), Ohm	Lm (115), mH	Rc, pu	Xm, pu	Lm, pu
0.108	10	9	0.3	1.111	333.333	96.386	306.806	260.848	75.426	240.089	78.895	22.813	22.813
0.131	20	17	1.2	1.176	333.333	171.745	546.681	260.848	134.398	427.802	78.895	40.650	40.650
0.154	30	26	2.6	1.154	346.154	235.667	750.150	270.881	184.420	587.026	81.930	55.779	55.779
0.172	40	35	4.2	1.143	380.952	293.618	934.615	298.112	229.769	731.378	90.166	69.495	69.495
0.190	50	44	6.2	1.136	403.226	347.323	1105.563	315.542	271.795	865.152	95.438	82.207	82.207
0.211	60	53	8.5	1.132	423.529	383.705	1221.372	331.431	300.267	955.778	100.244	90.818	90.818
0.234	70	62	11.1	1.129	441.441	406.790	1294.854	345.448	318.332	1013.281	104.483	96.282	96.282
0.264	80	71	14.0	1.127	457.143	404.728	1288.288	357.735	316.717	1008.142	108.199	95.793	95.793
0.302	90	80	17.3	1.125	468.208	386.388	1229.913	366.394	302.366	962.461	110.818	91.453	91.453
0.357	100	89	20.8	1.124	480.769	344.653	1097.066	376.223	269.707	858.503	113.792	81.575	81.575
0.437	110	98	24.8	1.122	487.903	293.841	935.326	381.806	229.944	731.934	115.480	69.548	69.548
0.545	120	107	29.2	1.121	493.151	246.072	783.272	385.912	192.562	612.945	116.722	58.242	58.242
0.692	130	116	34.1	1.121	495.601	203.011	646.205	387.830	158.865	505.684	117.302	48.050	48.050
			Avearge:	1.132	426.519	293.379	933.855	333.770	229.582	730.783	100.951	69.439	69.439

Table C4. Short-circuit test results and parameters of the series transformer T1

Short-circuit Test (T1)													
I (130), A	V (130), V	P, W	I (115),A	Zeq (130), Ohm	Req (130), Ohm	Xeq (130), Ohm	Leq (130), mH	Req (115), Ohm	Xeq (115), Ohm	Leq (115), mH	Req, pu	Xeq, pu	Leq, pu
1.172	0.30	0.3	1.325	0.256	0.218	0.133	0.425	0.171	0.104	0.333	0.052	0.032	0.032
2.062	0.52	0.8	2.331	0.252	0.188	0.168	0.534	0.147	0.131	0.418	0.045	0.040	0.040
3.216	0.81	2.0	3.635	0.252	0.193	0.161	0.514	0.151	0.126	0.402	0.046	0.038	0.038
4.245	1.07	3.4	4.799	0.252	0.189	0.167	0.532	0.148	0.131	0.416	0.045	0.040	0.040
5.083	1.29	4.9	5.746	0.254	0.190	0.169	0.537	0.148	0.132	0.420	0.045	0.040	0.040
6.238	1.58	7.3	7.052	0.253	0.188	0.170	0.542	0.147	0.133	0.424	0.044	0.040	0.040
7.105	1.79	9.5	8.032	0.252	0.188	0.167	0.533	0.147	0.131	0.417	0.045	0.040	0.040
8.283	2.10	13.0	9.363	0.254	0.189	0.168	0.536	0.148	0.132	0.420	0.045	0.040	0.040
9.203	2.33	16.0	10.403	0.253	0.189	0.169	0.537	0.148	0.132	0.420	0.045	0.040	0.040
10.146	2.56	19.4	11.469	0.252	0.188	0.168	0.534	0.147	0.131	0.418	0.045	0.040	0.040
11.083	2.80	23.1	12.529	0.253	0.188	0.169	0.537	0.147	0.132	0.420	0.045	0.040	0.040
12.010	3.03	27.1	13.577	0.252	0.188	0.168	0.536	0.147	0.132	0.419	0.044	0.040	0.040
13.242	3.35	33.0	14.969	0.253	0.188	0.169	0.538	0.147	0.132	0.421	0.045	0.040	0.040
14.015	3.55	37.1	15.843	0.253	0.189	0.169	0.537	0.148	0.132	0.420	0.045	0.040	0.040
15.110	3.82	43.1	17.081	0.253	0.189	0.168	0.535	0.148	0.132	0.419	0.045	0.040	0.040
16.200	4.10	49.6	18.313	0.253	0.189	0.168	0.536	0.148	0.132	0.419	0.045	0.040	0.040
17.280	4.36	56.2	19.534	0.252	0.188	0.168	0.535	0.147	0.132	0.419	0.045	0.040	0.040
18.205	4.59	62.4	20.580	0.252	0.188	0.168	0.534	0.147	0.131	0.418	0.045	0.040	0.040
19.171	4.83	69.2	21.672	0.252	0.188	0.167	0.533	0.147	0.131	0.417	0.045	0.040	0.040
20.020	5.07	76.1	22.631	0.253	0.190	0.168	0.533	0.149	0.131	0.417	0.045	0.040	0.040
21.252	5.39	85.7	24.024	0.254	0.190	0.168	0.536	0.148	0.132	0.419	0.045	0.040	0.040
22.212	5.63	93.5	25.109	0.253	0.190	0.168	0.536	0.148	0.132	0.419	0.045	0.040	0.040
23.080	5.85	101.2	26.090	0.253	0.190	0.168	0.534	0.149	0.131	0.418	0.045	0.040	0.040
24.245	6.16	112.1	27.407	0.254	0.191	0.168	0.534	0.149	0.131	0.418	0.045	0.040	0.040
25.480	6.48	124.0	28.803	0.254	0.191	0.168	0.535	0.149	0.131	0.418	0.045	0.040	0.040
			Avearge:	0.253	0.190	0.167	0.530	0.149	0.130	0.415	0.045	0.039	0.039

Fig.B6. Working UPQC

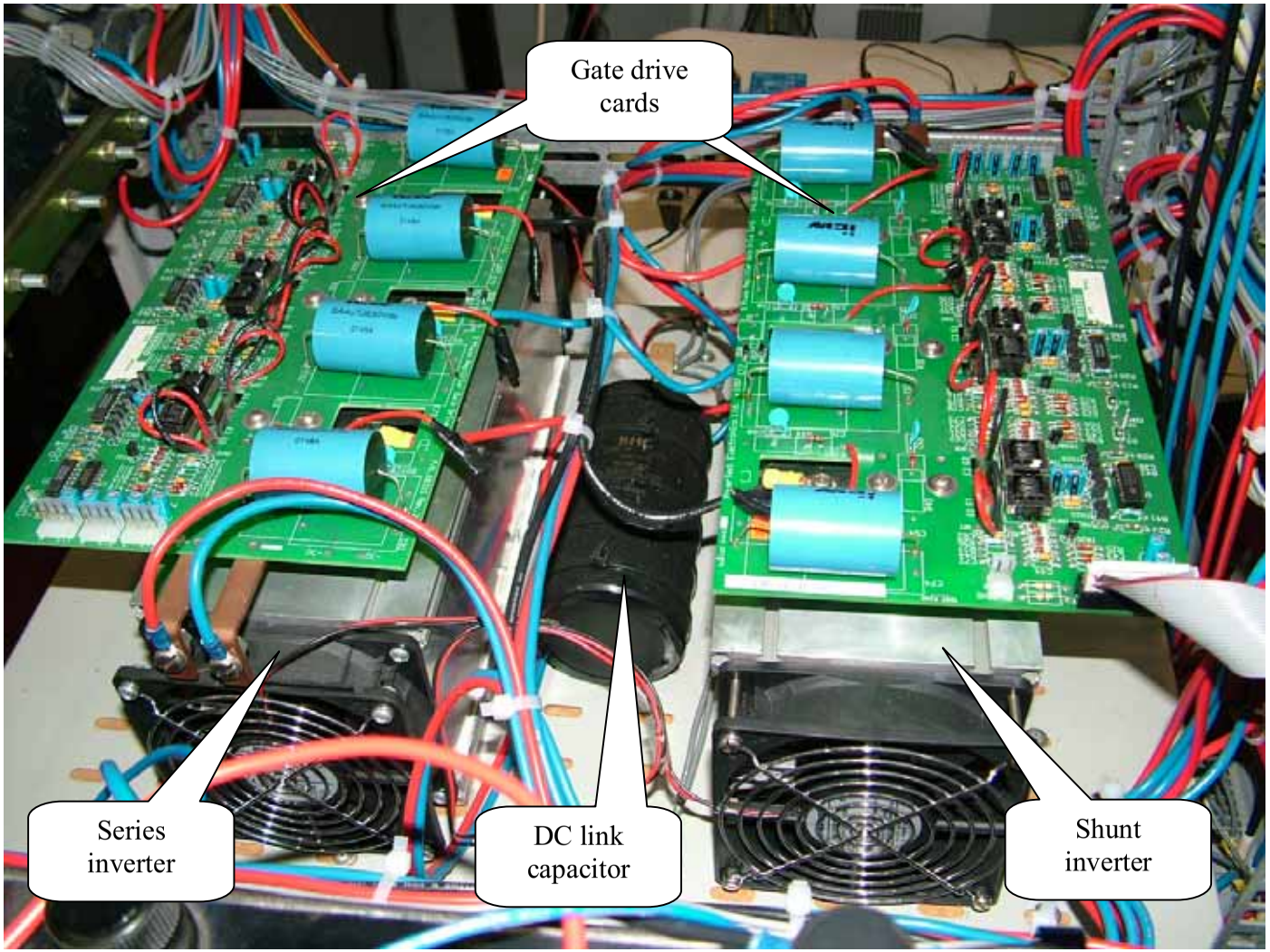


Fig.B5. Inverters

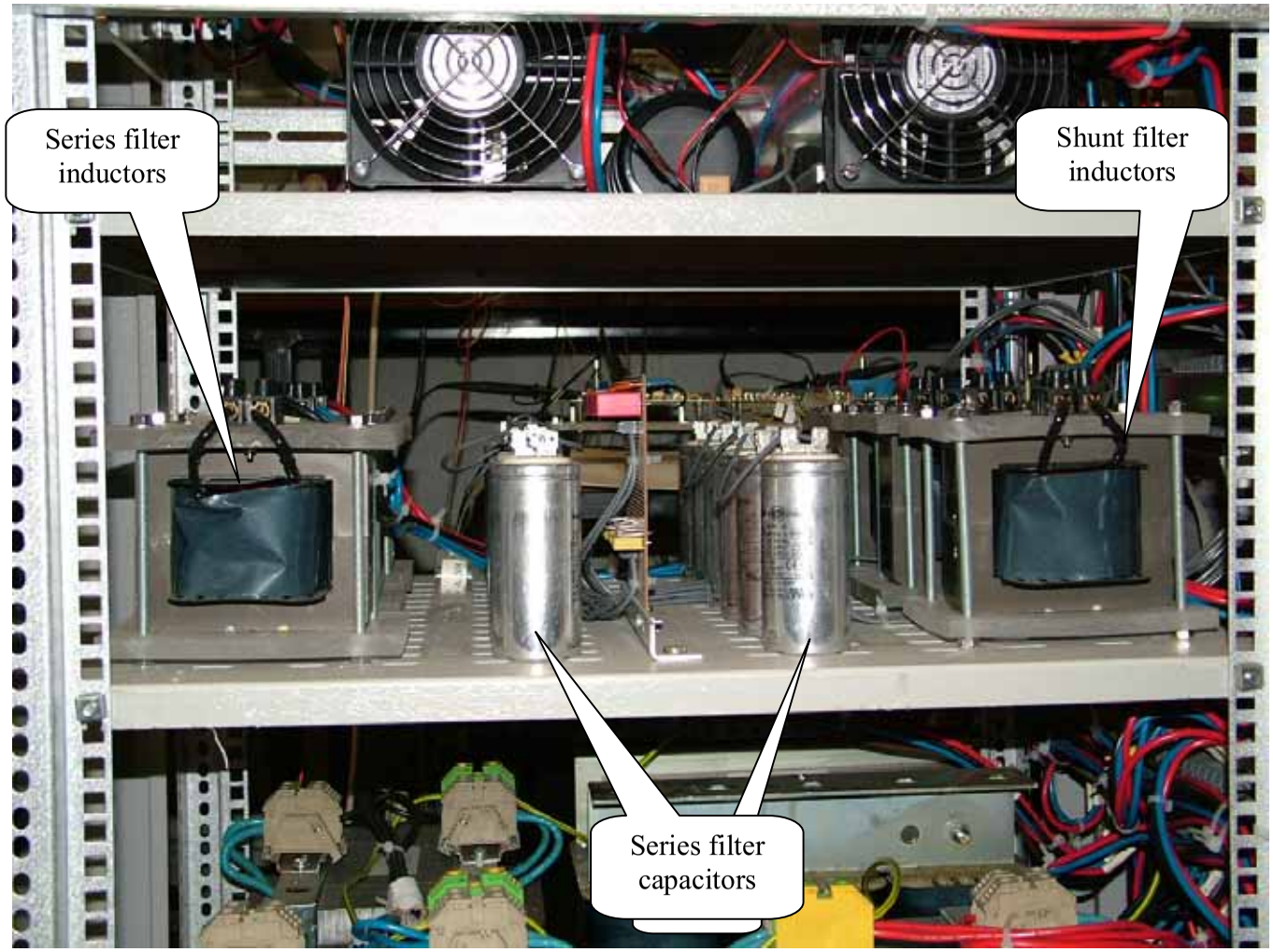


Fig.B4. Filtering inductors and capacitors

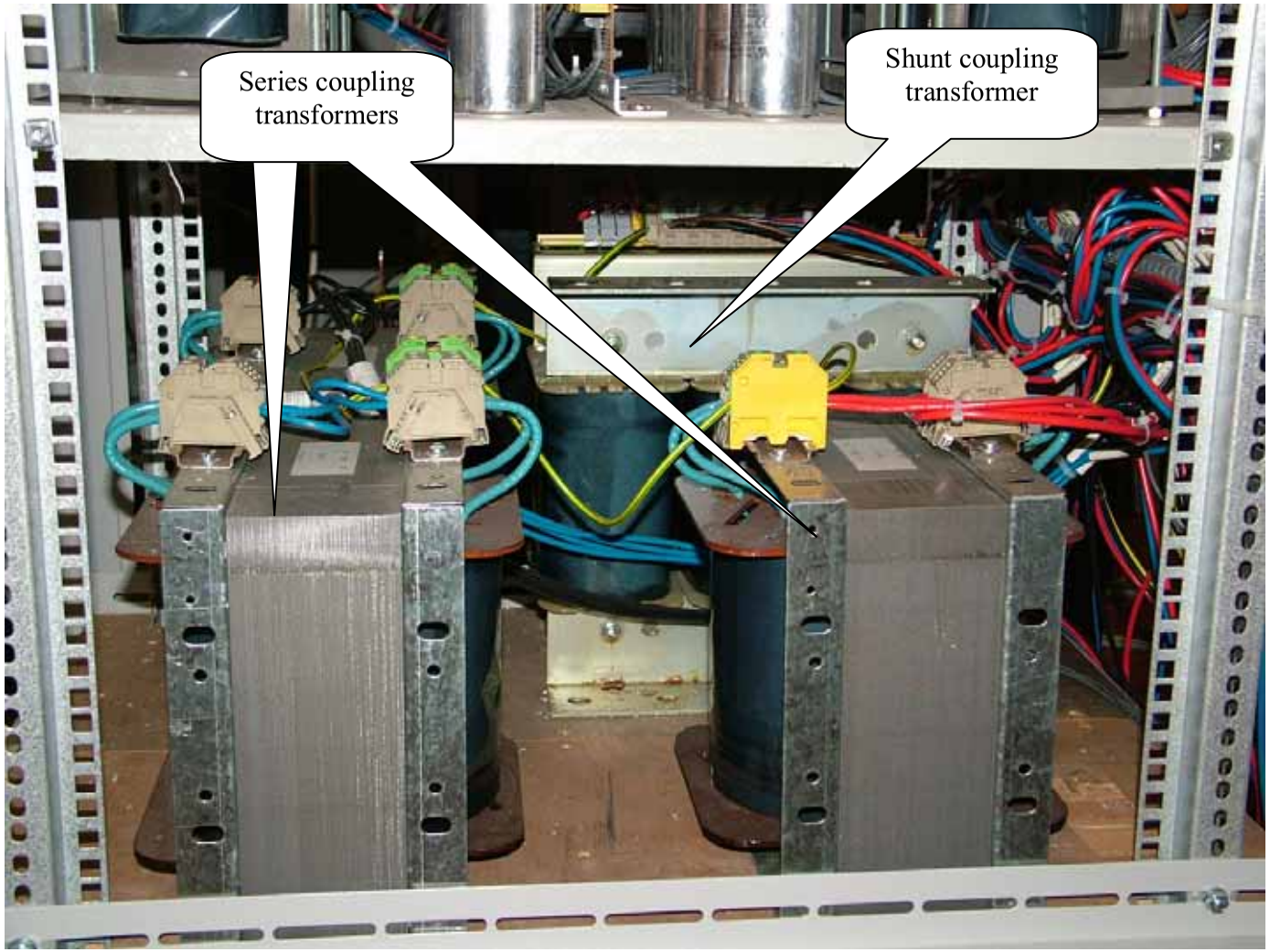


Fig.B3. Coupling transformers

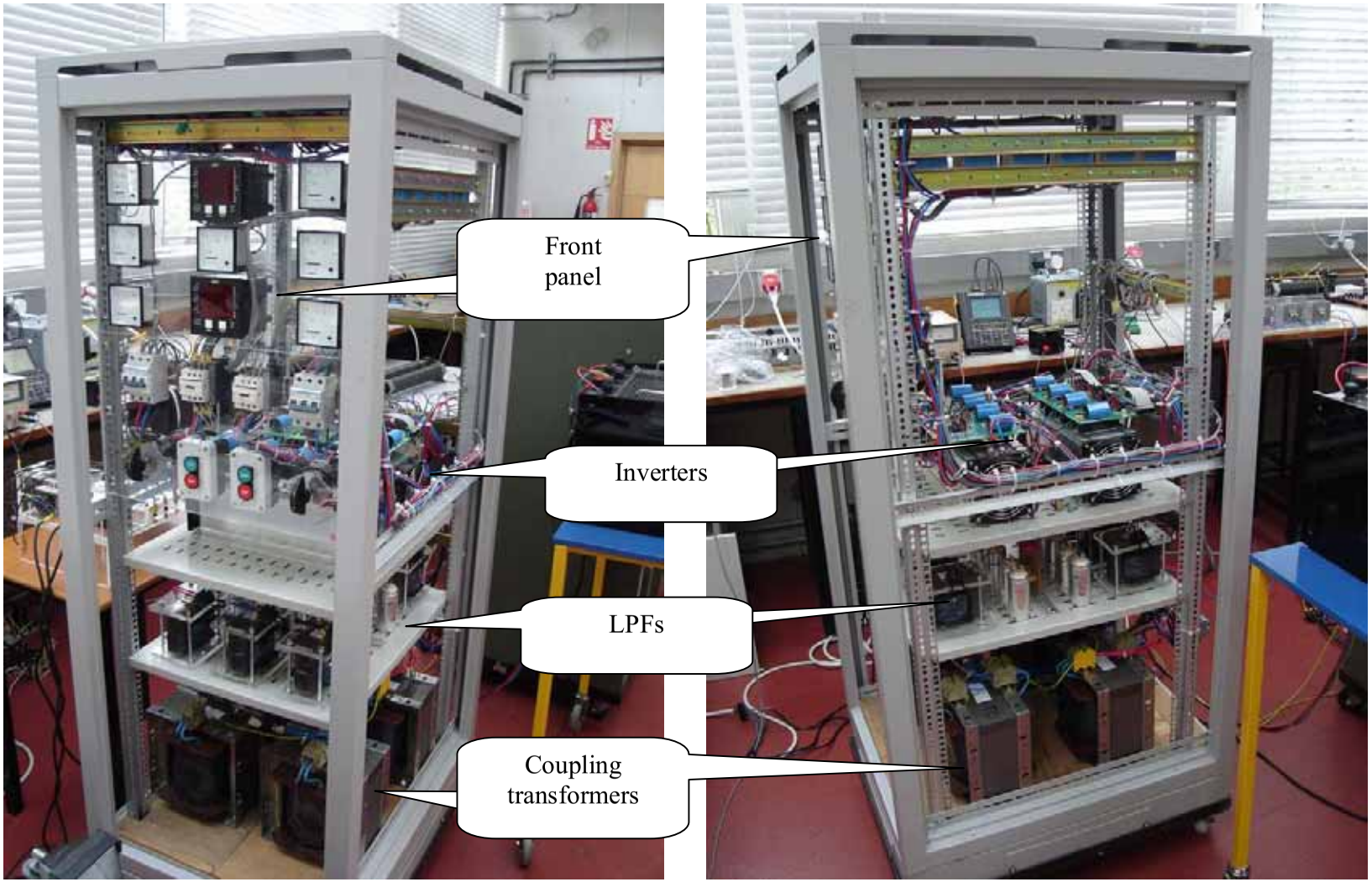


Fig.B2. Half-built prototype UPQC

Appendix B. Pictures of the prototype UPQC at different stages of construction

Fig.B1. Prototype UPQC at the beginning of construction

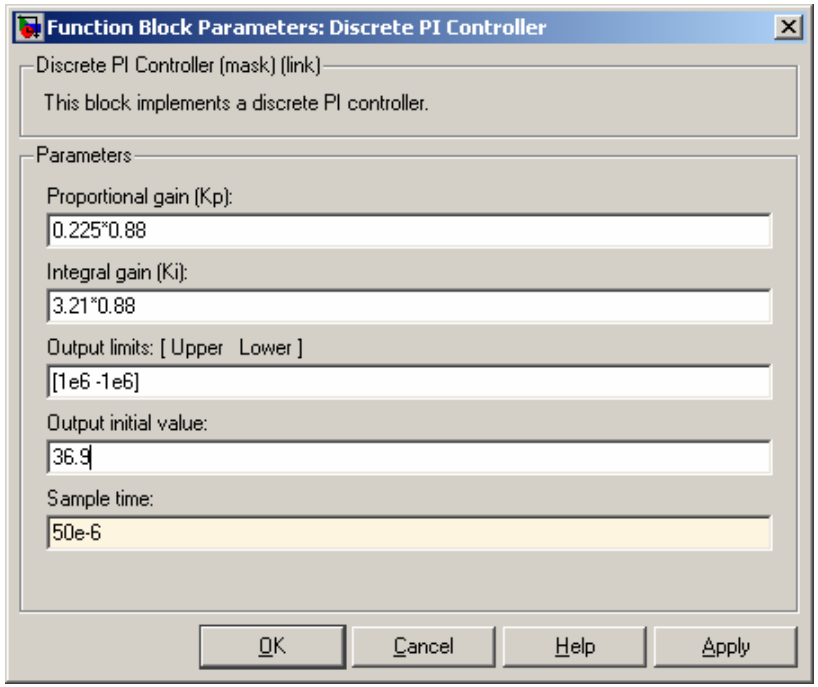


Fig.A27. PI controller parameters

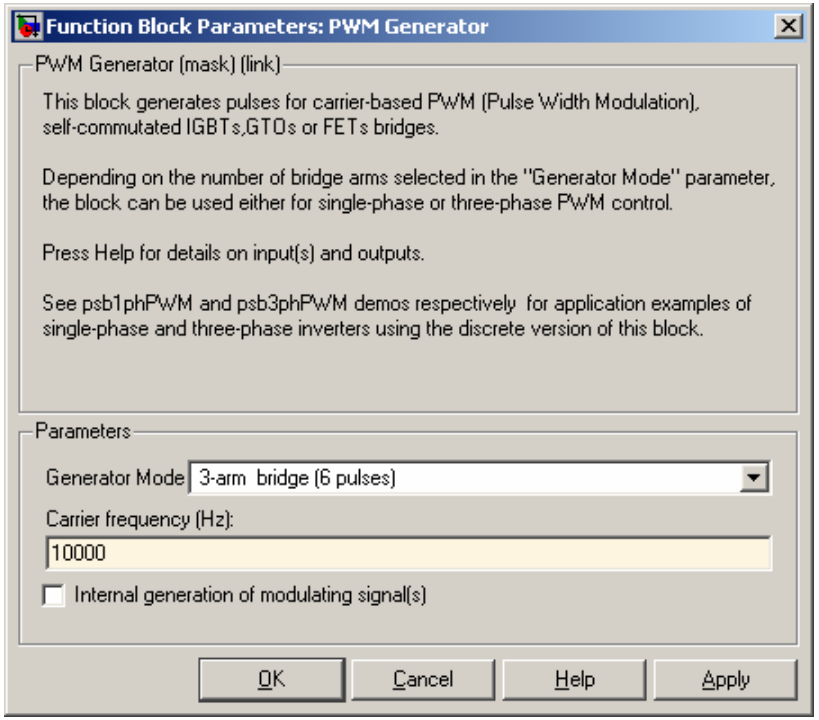


Fig.A28. Series PWM generator parameters

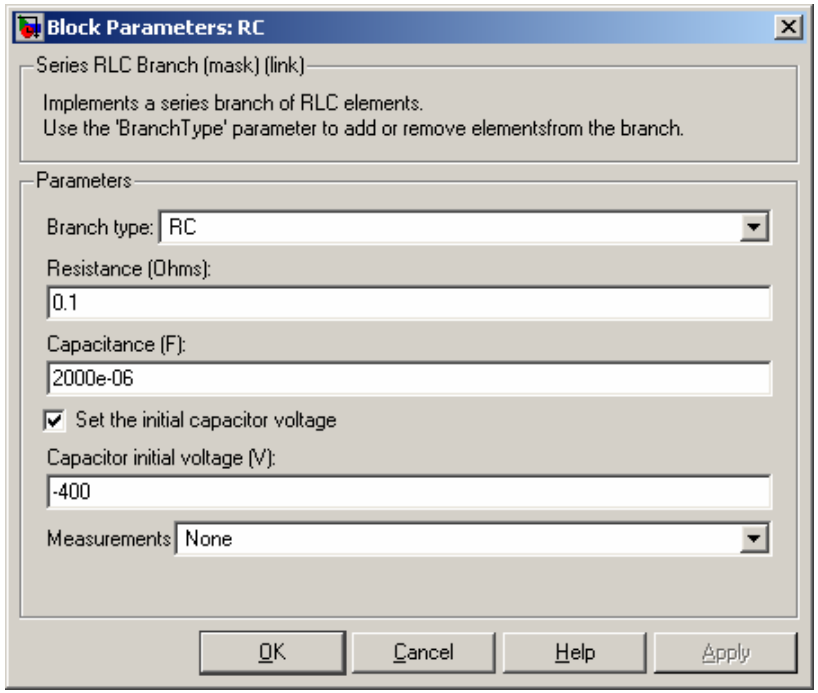


Fig.A25. DC link capacitor parameters

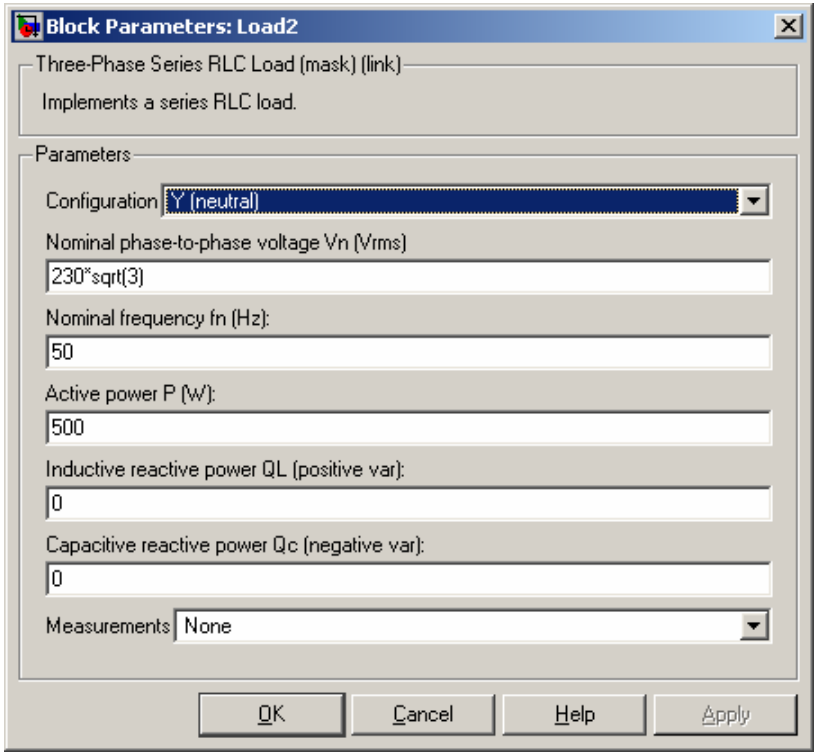


Fig.A26. Load2 parameters

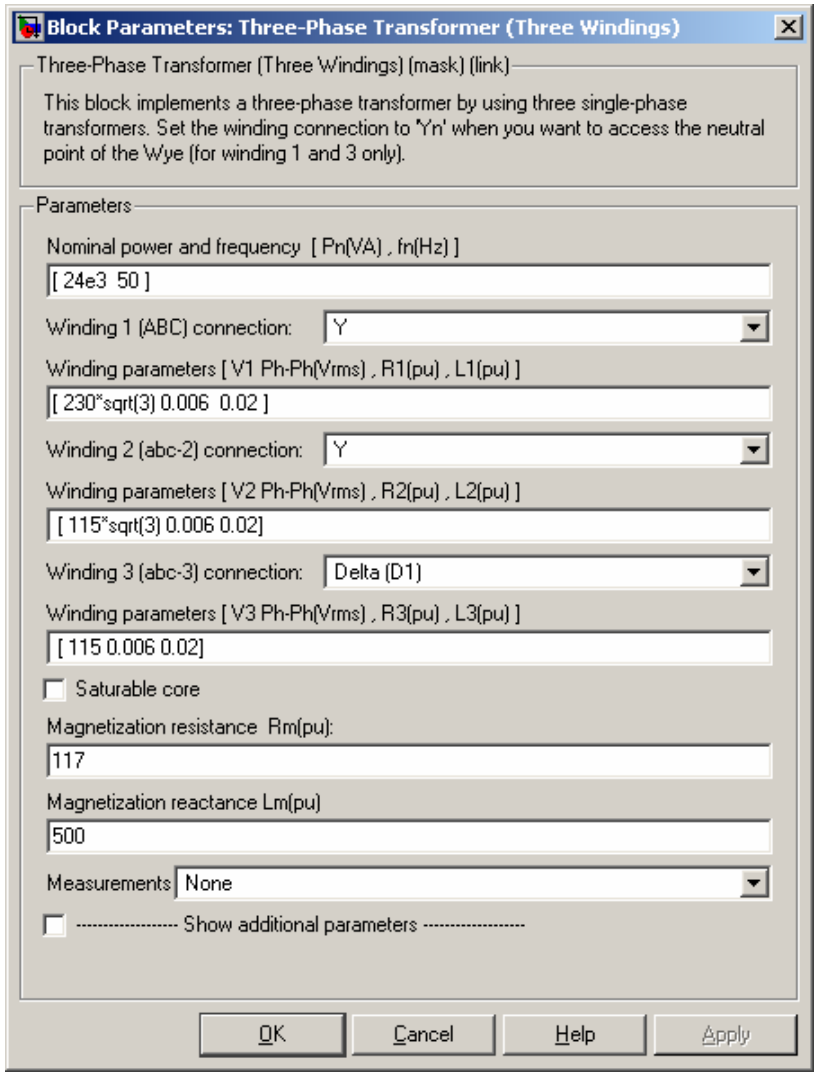


Fig.A23. Load transformer parameters

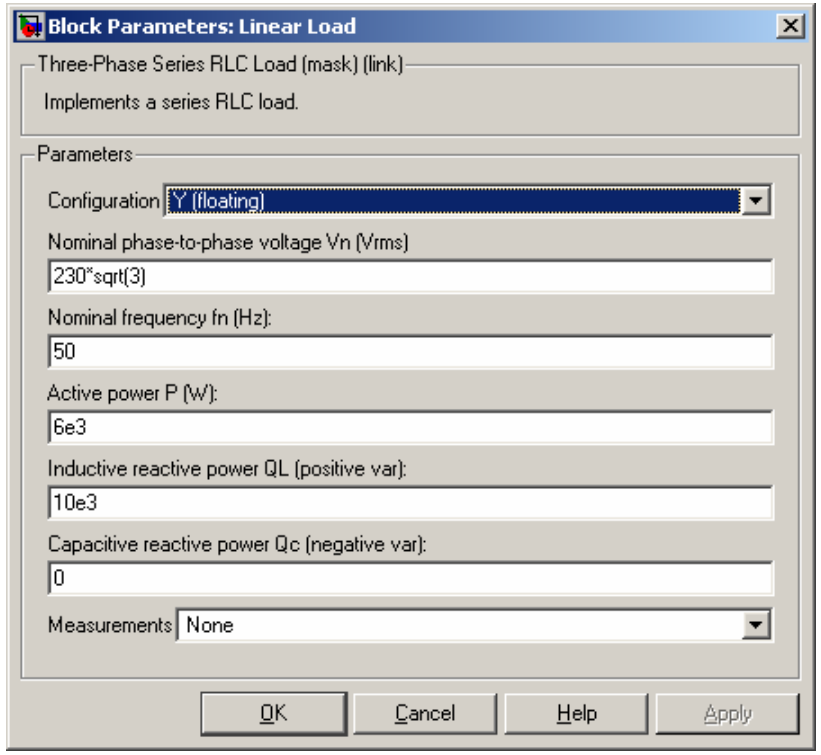


Fig.A24. Linear load parameters

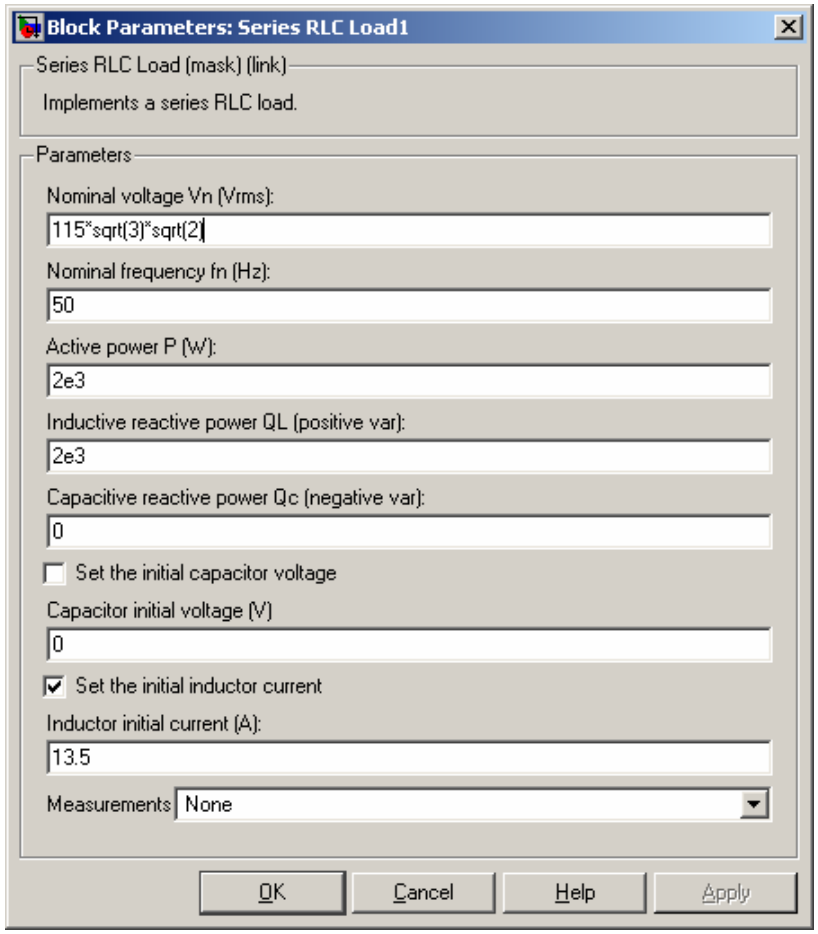


Fig.A21. Series RLC Load1 parameters

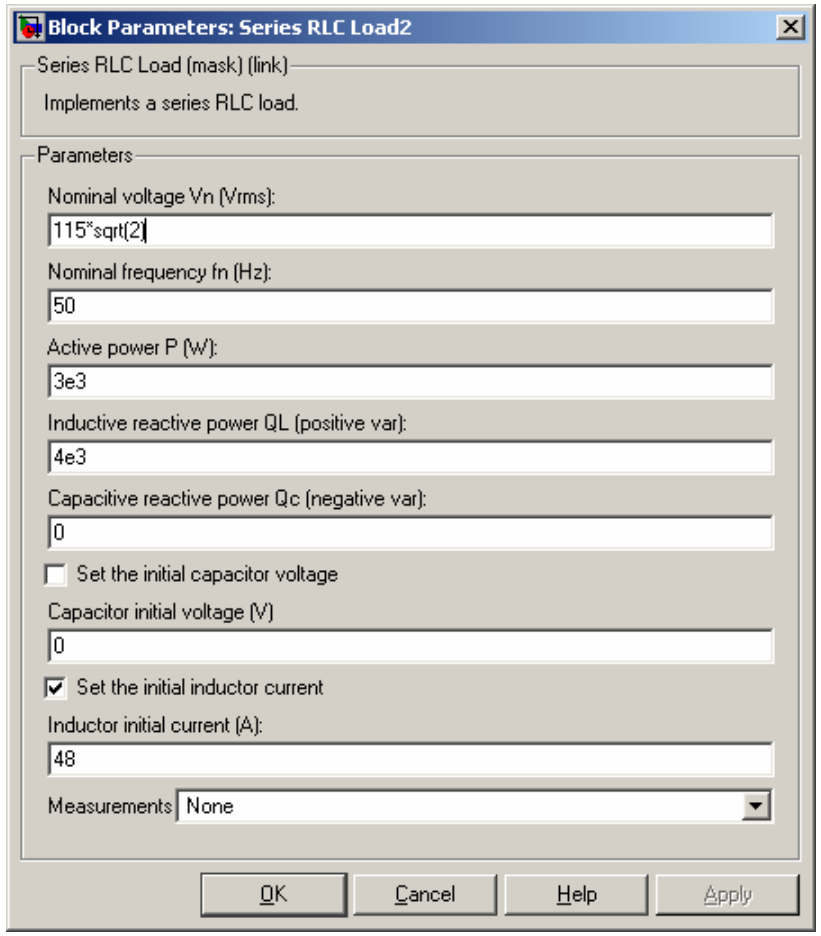


Fig.A22. Series RLC Load2 parameters

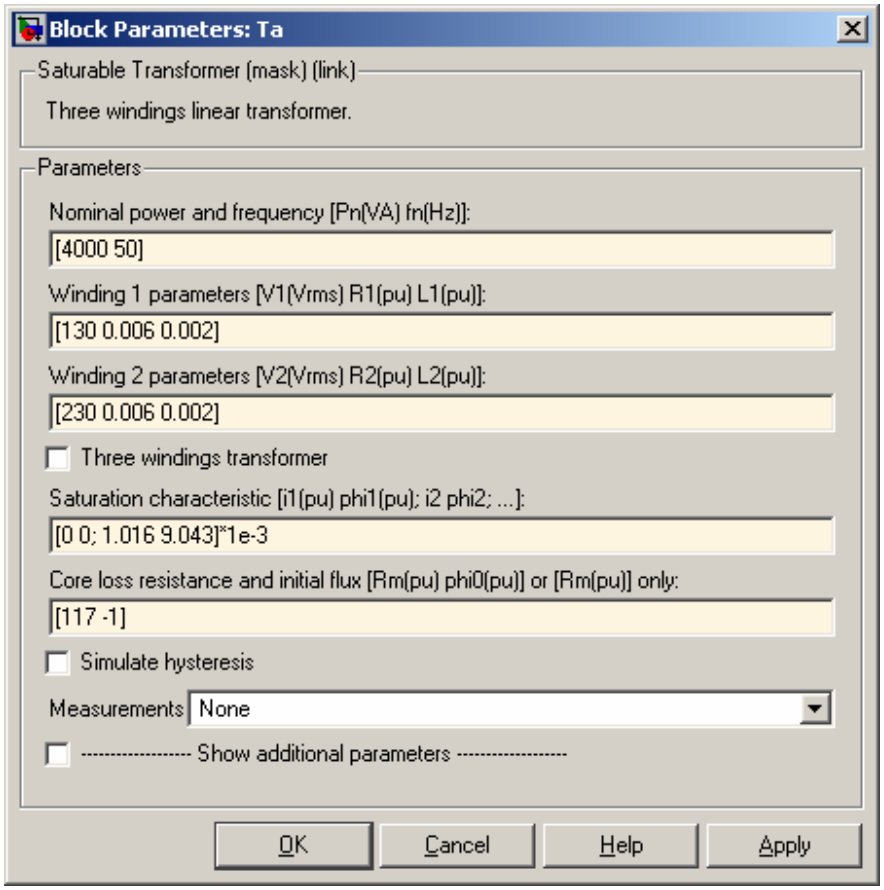


Fig.A19. Shunt coupling transformer parameters

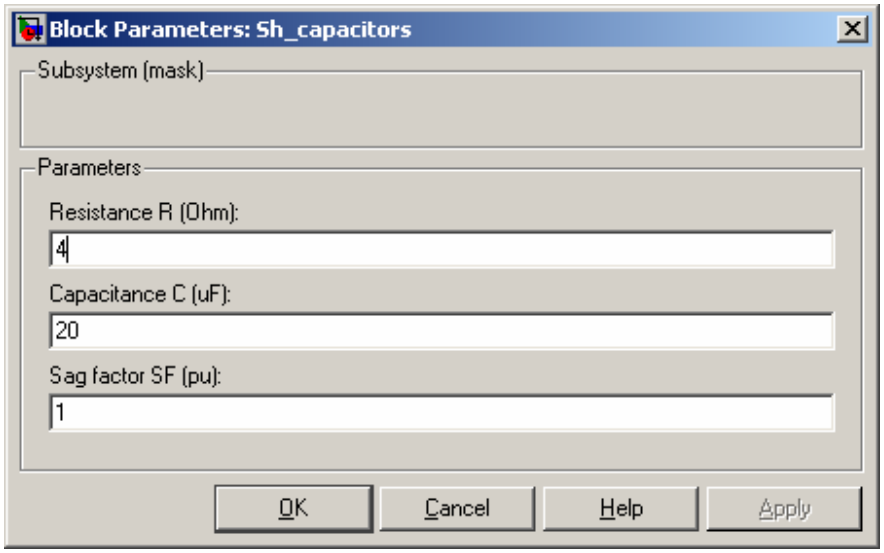


Fig.A20. Shunt capacitor parameters

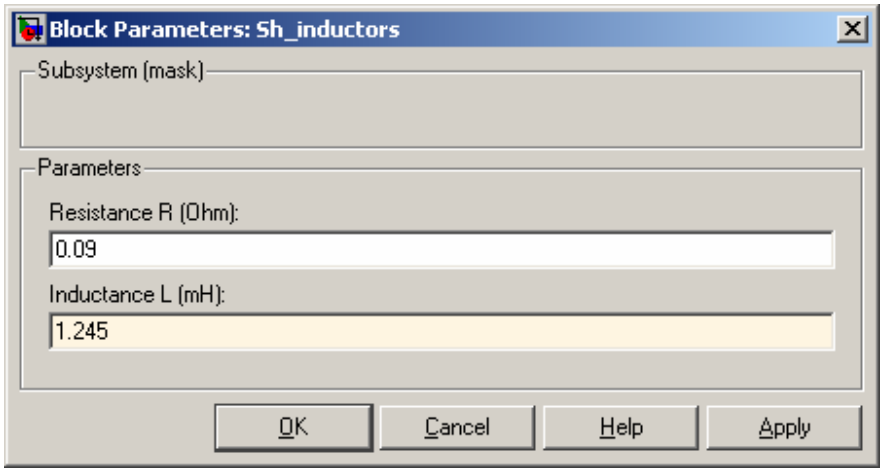


Fig.A17. Shunt inductor parameters

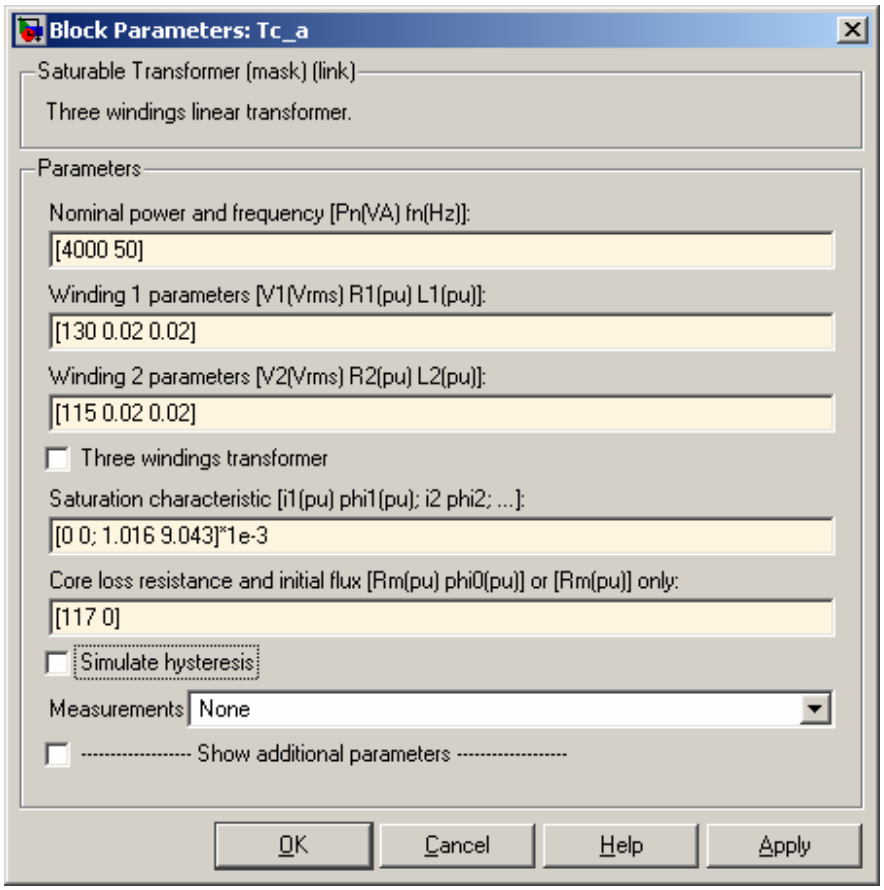


Fig.A18. Series coupling transformer parameters

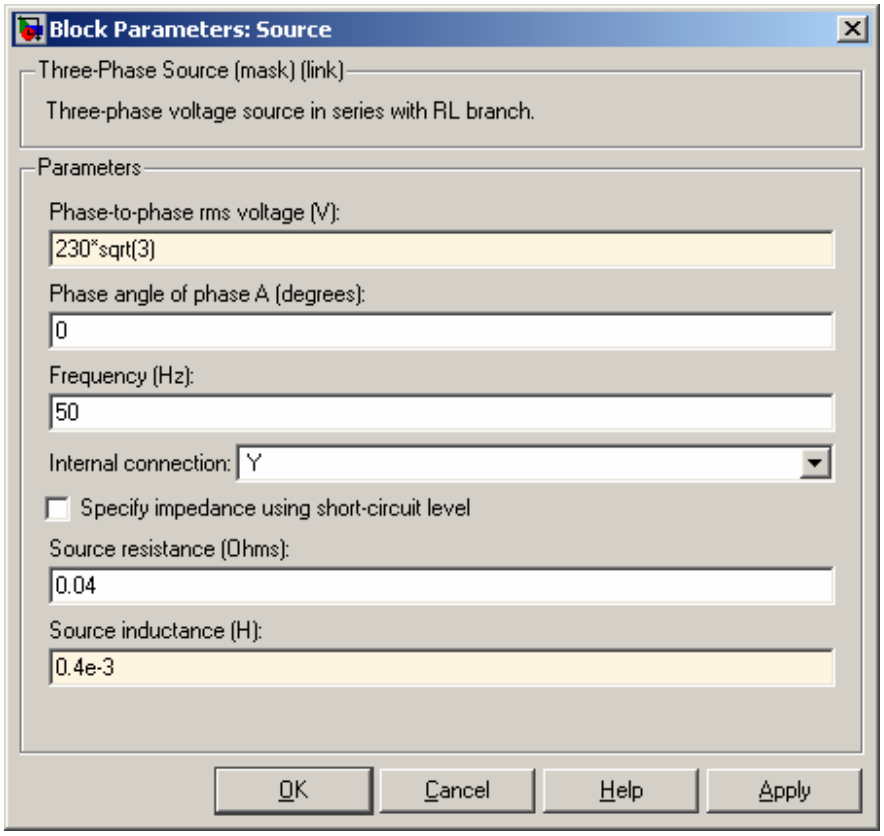


Fig.A15. Source parameters

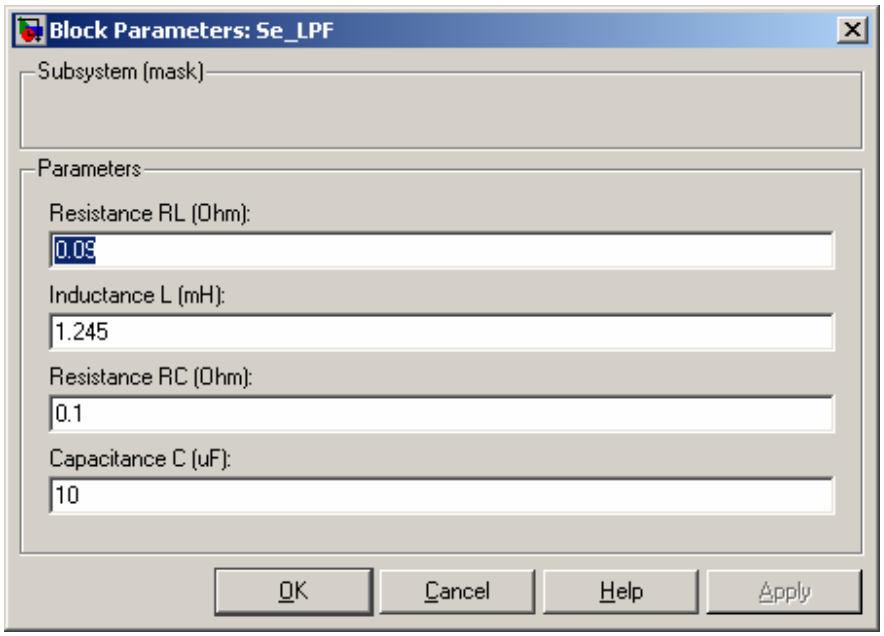


Fig.A16. Series LPF parameters

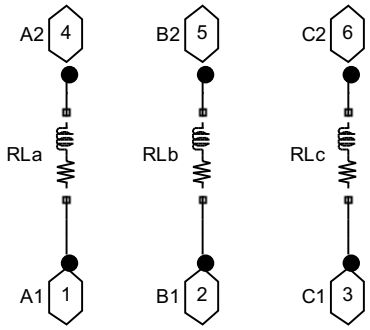


Fig.A12. Sh_inductors Subsystem

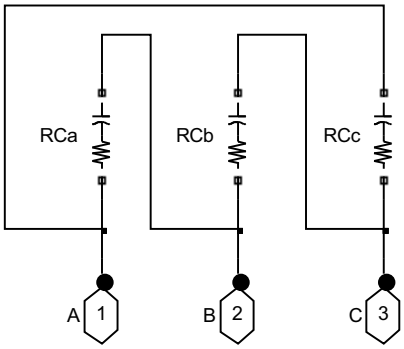


Fig.A13. Sh_capacitors Subsystem

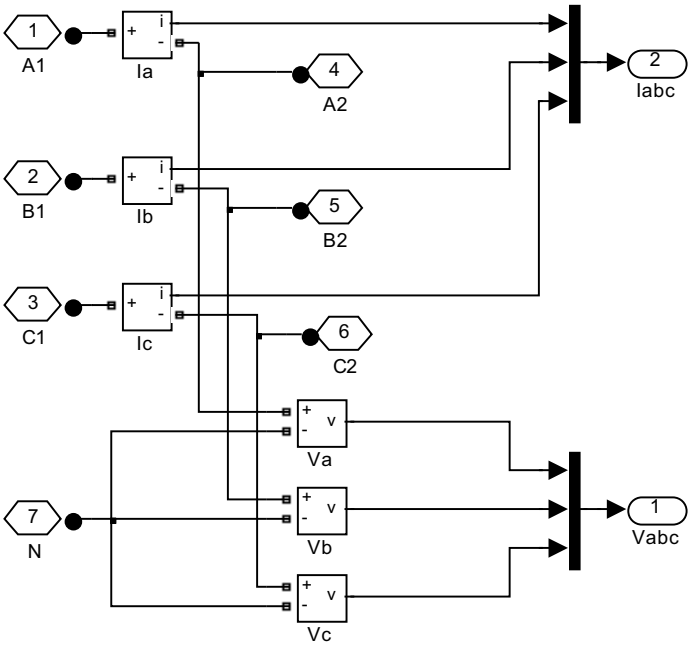


Fig.A14. Measurement Subsystem

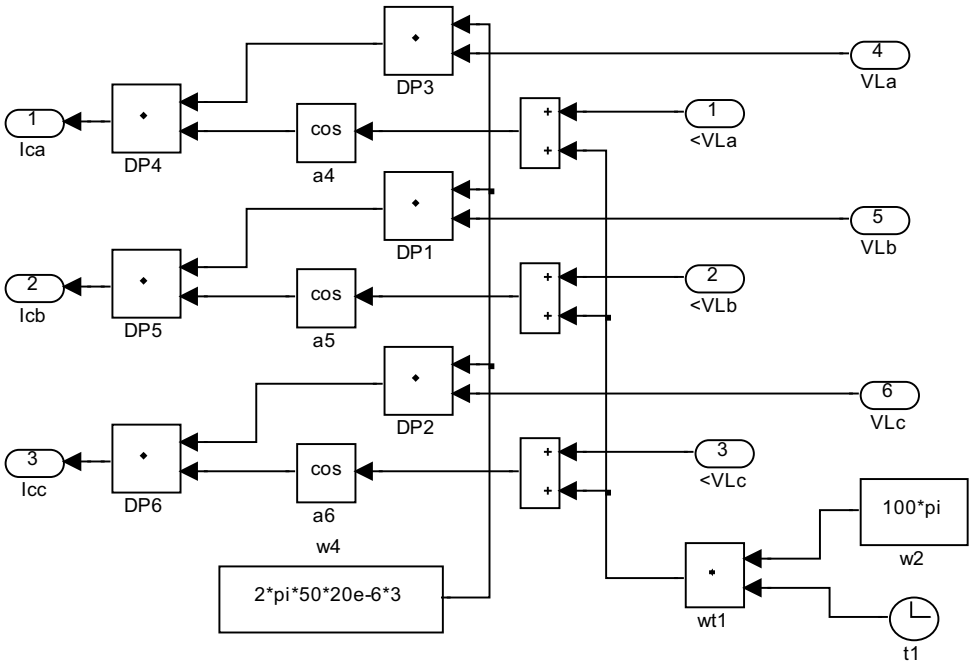


Fig.A10. C current Subsystem

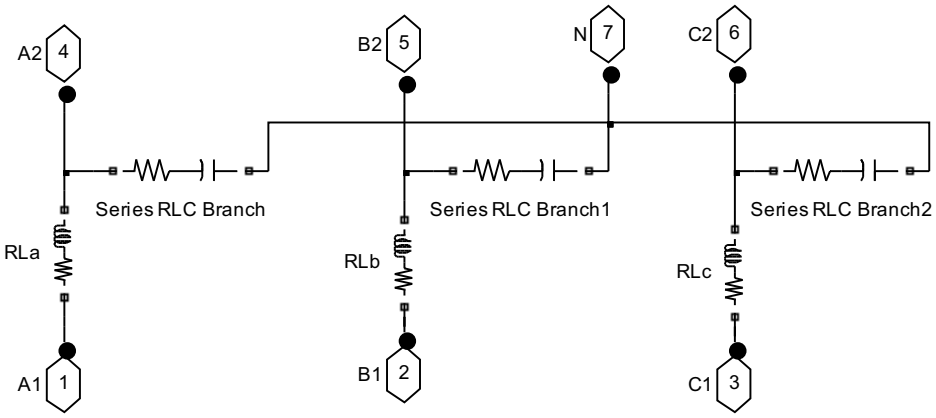


Fig.A11. Se_LPF Subsystem

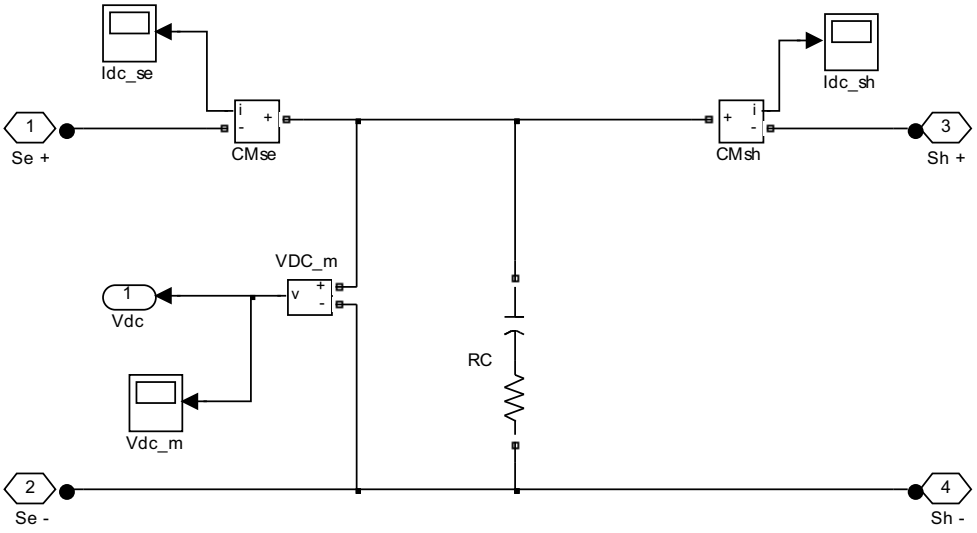


Fig.A8. DC Link Subsystem

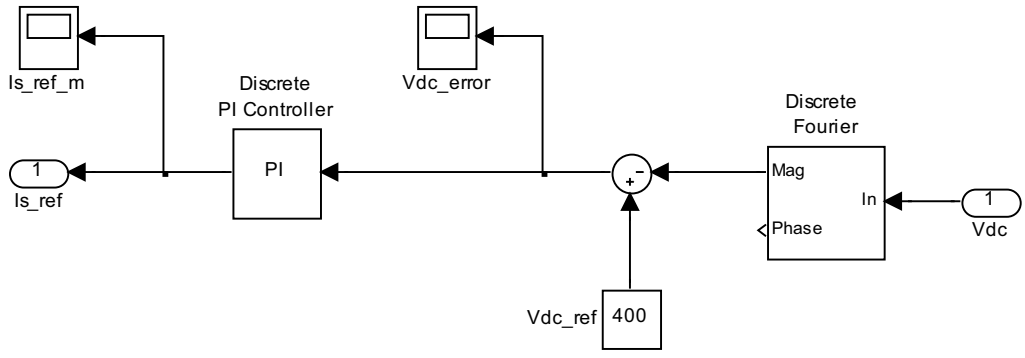


Fig.A9. DC link controller Subsystem

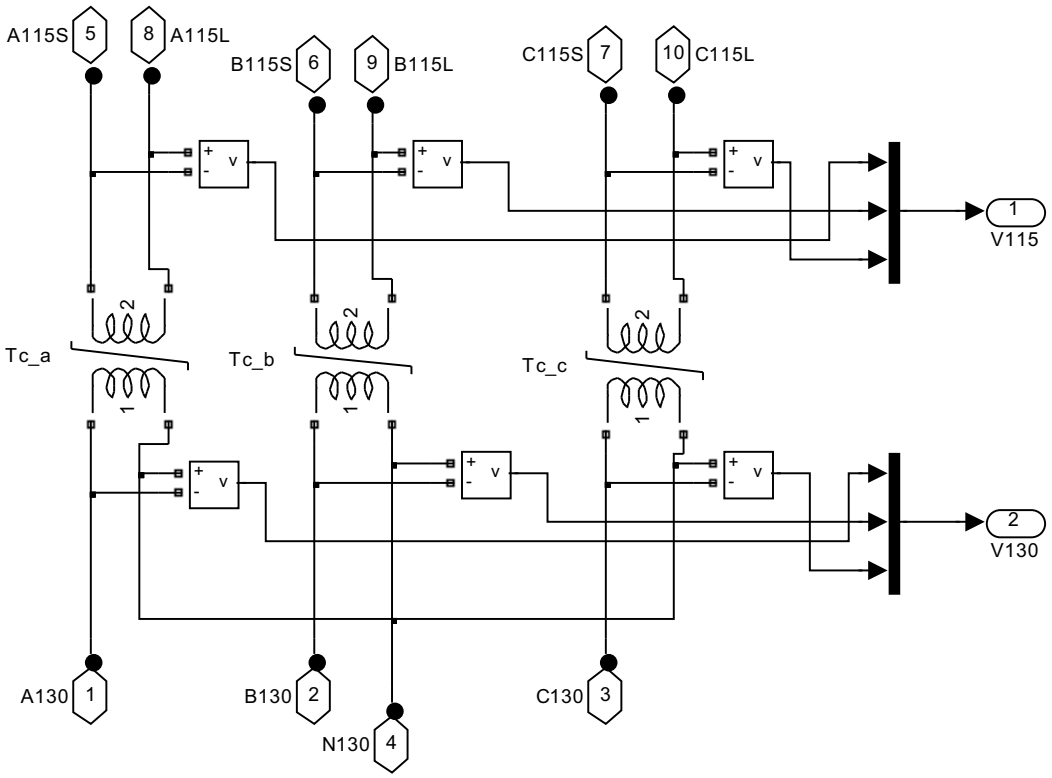


Fig.A6. Se_transf Subsystem

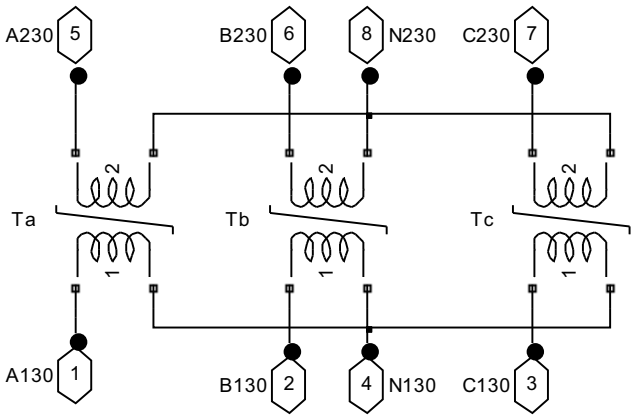


Fig.A7. Sh_transf Subsystem

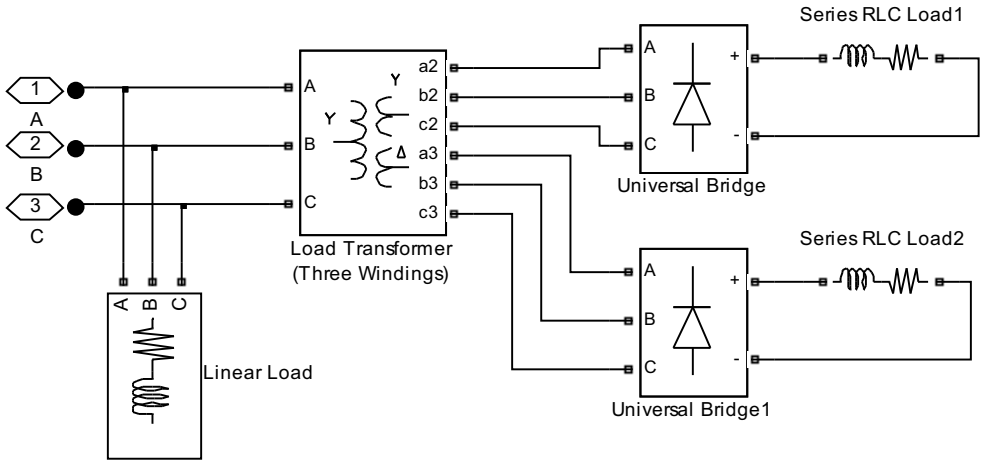


Fig.A4. Load Subsystem

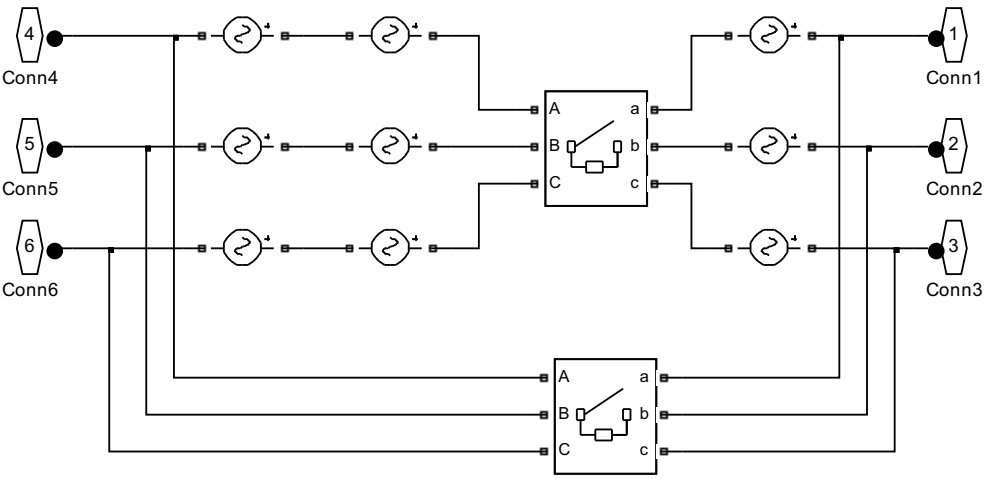


Fig.A5. Unb_Dist_creation Subsystem

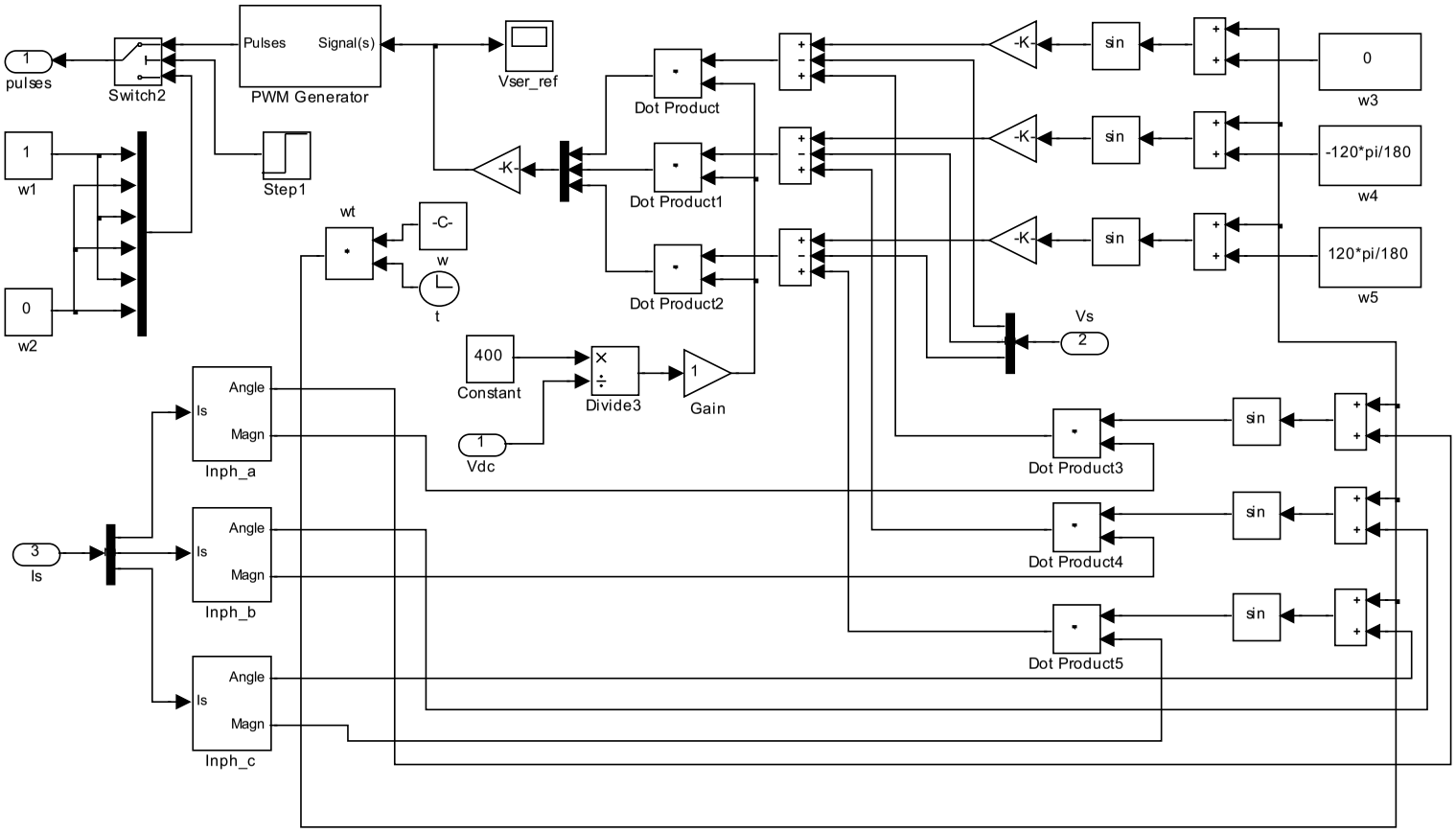


Fig.A3. Series compensator control block

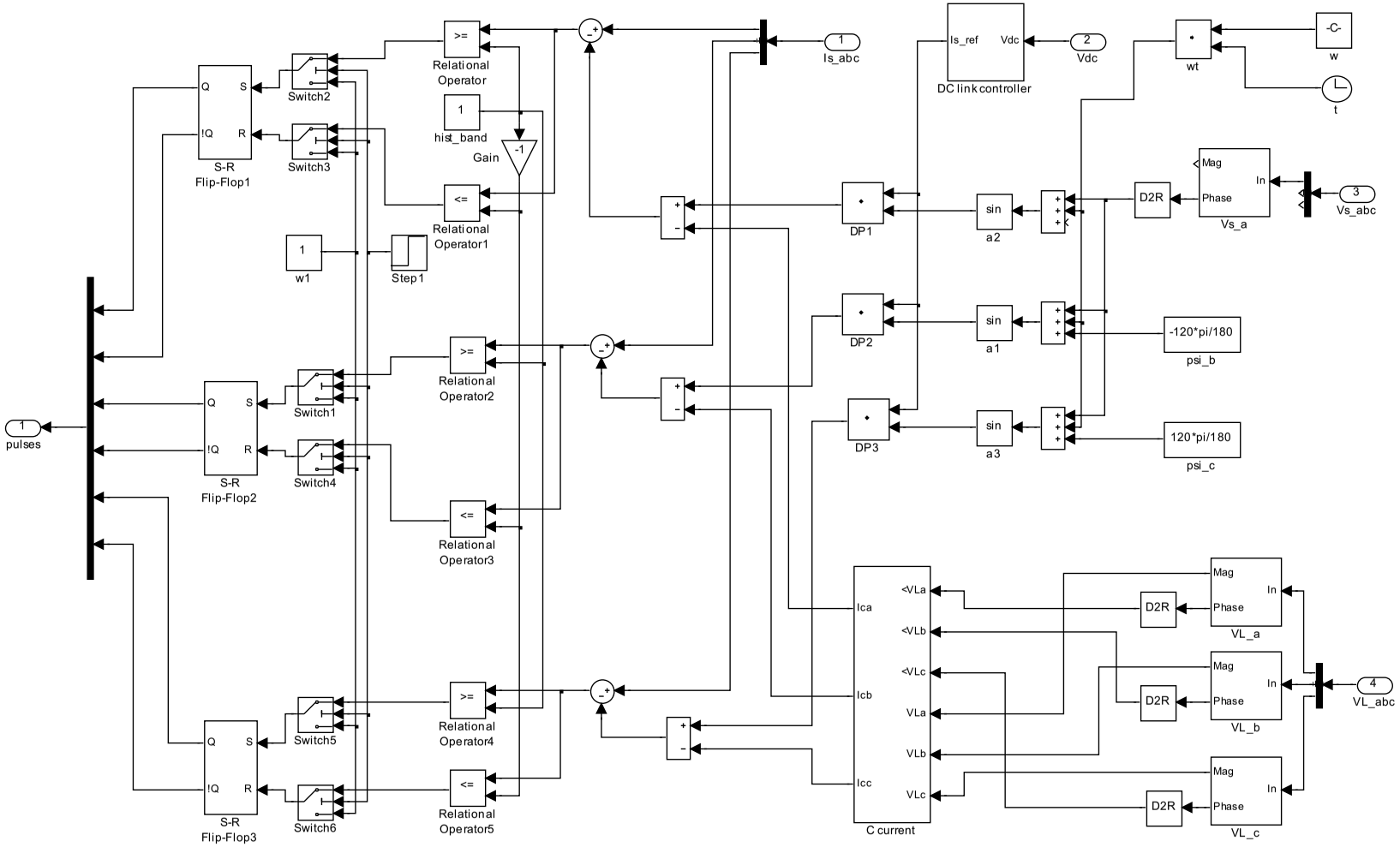


Fig.A2. Shunt compensator control block

Appendix A. UPQC simulation model created in Matlab/Simulink

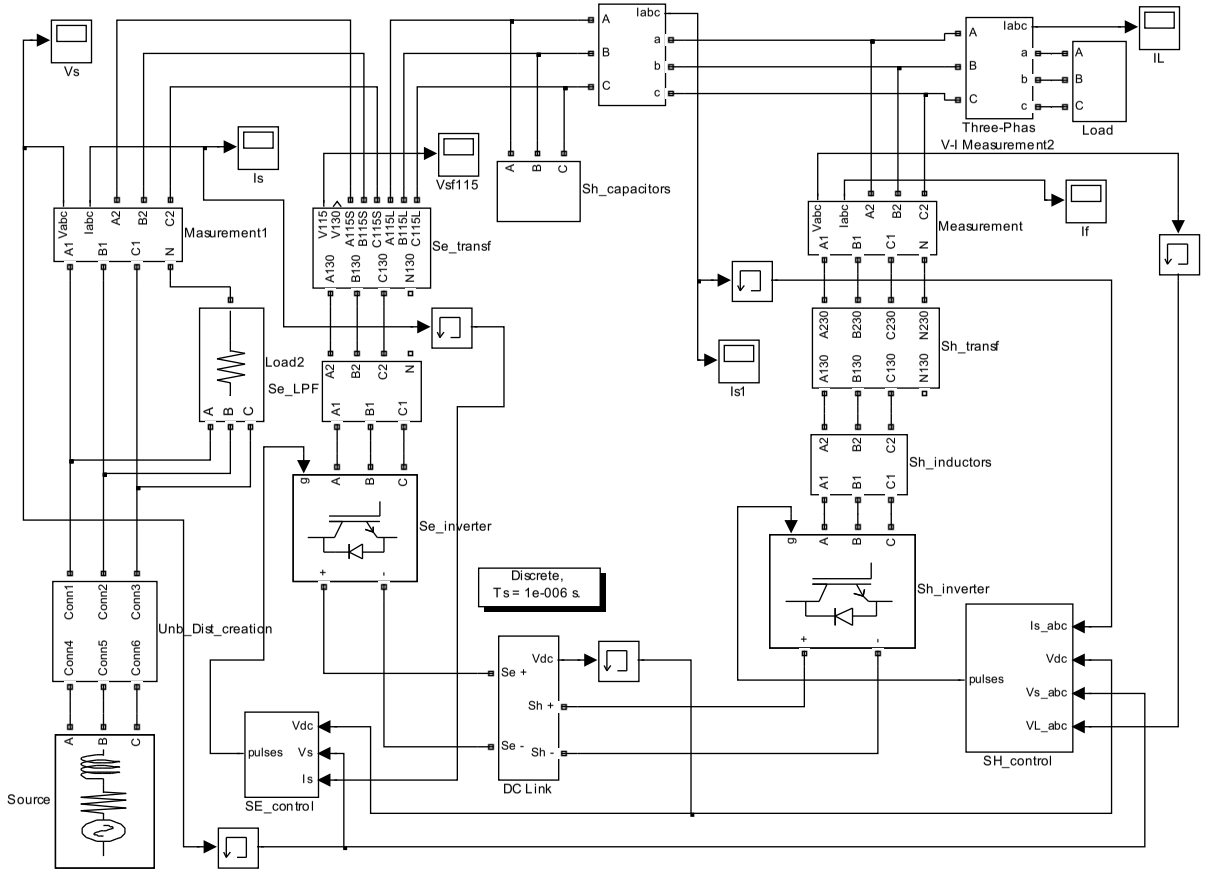


Fig.A1. UPQC power circuit

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5. In this research, the basic inverter has been considered which has a switching frequency, voltage rating and power capacity limited by the rating of individual switches. Combining many switches can address one or more of the inverter limitations. Thus, the UPQC configurations employing multi-step and multilevel inverter topologies must be investigated.
6. In a higher rating UPQC, the protection crowbar proposed in Chapter 4 will employ high rating thyristors which require substantially higher gate currents. Therefore, the control circuit proposed in Chapter 4 has to be modified to meet the gate current requirements. Since the Zener diode current carrying capability is limited, some effective current amplification solutions have to be searched.

7.2. Future work

There are several important points, which need to be investigated but could not constitute the scope of this research work due to its limited time frame. Thus, during the course of this research, the following issues have been identified as possibly topics for future work in this area:

1. This research can be extended to investigate the 3-phase 4-wire UPQC;
2. The control techniques proposed in Section 5.3 and Chapter 6 have been verified through simulations. The implementation of these control techniques in a DSP based control scheme and experimental validation of their effectiveness is the next step;
3. Since the turn on/off instances of the inverter complementary switches are delayed by a blanking time, the voltage injected by the series compensator contains unwelcome low frequency harmonics. A special control technique has to be implemented for minimizing the undesirable effects of blanking time;
4. In Section 5.2.1, it is suggested that the resonance at switching frequencies of the shunt filter capacitor with the feeder inductance is avoided by proper choice of switching frequency and introducing a small value damping resistor in series with the shunt filter capacitor. However, this solution requires additional hardware and causes additional losses. The resonance can also be avoided by applying an appropriate control action to the series compensator. Thus, some investigations in this direction are required.

voltage generated by the shunt inverter. The appropriate control block has been derived and the effectiveness of this approach has been proved through simulations.

The load change, as well as supply voltage sag/swell occurrence/clearance causes the dc link voltage deviations. In turn, this causes deviations in the voltage injected by the series compensator, hence in the load voltage. In order to overcome this problem two complementary control strategies have been proposed and investigated. The first control strategy deals with the series inverter and it consists in continuous adjustment of the amplitude modulation ratio. It has been proposed that the amplitude modulation ratio of the series inverter is continuously adjusted to match the actual dc link voltage rather than the reference dc link voltage. The second control strategy deals with the dc link voltage controller. An adaptive dc link voltage controller has been proposed for obtaining a better performance system both in steady state and during the transients. During the steady state operation, a LPF with 50 Hz cut-off frequency is used and the corresponding PI controller parameters are applied. In transient conditions, a LPF with 300 Hz cut-off frequency and the corresponding PI controller parameters are applied. The effectiveness of the proposed control strategies has been proved trough simulations.

It is hoped that theoretical as well as experimental investigations reported in this thesis will help in establishing new topological designs and control schemes for active power compensators in an attempt to improve the power quality. It is further hoped that application engineers will be able to utilize the results reported in this thesis for further enhancement of compensator performance under adverse load and supply conditions.

The proposed protection scheme is simple to implement and it does not interfere with the upstream protection installed in power distribution system. Its effectiveness has been confirmed through simulations carried out in Simulink for different fault and system conditions. It has been shown that using the proposed protection scheme the series inverter is fully protected from both overcurrent and overvoltage, and the overall reliability of the equipment is enhanced. Also, an experimental overvoltage protection circuit has been designed, built, tested and incorporated into the UPQC laboratory prototype. Thus, the effectiveness of the proposed protection scheme has also been validated through experiments.

In situations where the UPQC is connected to a weak supply point and a hysteresis band controller is used to control the shunt inverter, due to the switching frequencies in the supply current, the load side voltage can become unacceptably distorted. Therefore, LC or/and LCL filters are used to interface the shunt inverter with the distribution network. Although this prevents the switching frequency components generated by the shunt inverter from entering into the grid, it involves more complex control techniques to maintain the system stability. However, because of its simplicity, the hysteresis based control strategy is very attractive from the practical implementation point of view. Thus, a control approach for avoiding the stability problem while using the hysteresis controller has been proposed and investigated. It has been shown both through simulations and experiments that if the "not filtered" supply current is tracked, rather than the supply current after filtering, the stability is maintained using the hysteresis band controller. As an alternative to hysteresis band controller it has been proposed to operate the shunt inverter in voltage control mode, in which case the shunt compensator current is controlled indirectly by controlling the

Chapter 7

CONCLUSIONS AND FUTURE WORK

7.1. Conclusions

The main objective of this research was to develop the UPQC protection scheme and control algorithms for enhanced performance. The objectives laid down for this PhD thesis have been successfully realized through analytical, simulation and experimental investigations. As part of this research activity, a 12 kVA prototype UPQC has been constructed and tested. Also, a UPQC simulation model has been built in Simulink, which greatly assisted in designing the prototype UPQC and developing new control solutions. The effectiveness of the UPQC has been proved through numerous simulation and experimental results.

A protection scheme for the series inverter has been proposed and investigated. This scheme protects the series inverter from overcurrents and overvoltages, which appear during a short circuit on the load side of UPQC. The main protection element is a crowbar connected across the secondary of the series transformer. As soon as an overvoltage appears the crowbar short-circuits the secondary of the transformer, thus removing the overvoltage and diverting the fault current from the series inverter. The overvoltage protection crowbar consists of a pair of antiparallel connected thyristors governed by a very simple Zener diode based control circuit, which does not require separate power source. In addition an overcurrent detector is used to disable the inverters in overcurrent conditions.

overcome this problem two complementary control strategies have been proposed and investigated.

The first control strategy deals with the series inverter controller and it consists in continuous adjustment of the amplitude modulation ratio. It is proposed that the amplitude modulation ratio m_a of the series inverter sinusoidal PWM voltage controller is continuously adjusted to match the actual dc link voltage rather than the reference dc link voltage. This compensation technique can be easily implemented both in DSP based and analog control schemes.

The second control strategy deals with the dc link voltage controller. An adaptive dc link voltage controller is proposed for obtaining a better system performance both in steady state and during the transients. During the steady state operation, a LPF with 50 Hz cut-off frequency is used and the corresponding PI controller parameters are applied. In transient conditions, a LPF with 300 Hz cut-off frequency and the corresponding PI controller parameters are applied. This compensation technique can be easily implemented in a DSP based controller.

The effectiveness of the proposed control strategies has been proved through simulations.

In Fig.6.12.b the supply currents are shown. Since during this transient the cut-off frequency of LPF is 300 Hz the supply currents are distorted (the magnitude varies), but this distortion only lasts for about 0.52 s. At 1.025 s the controller switched to steady-state parameters and from this point the supply currents are no longer distorted.

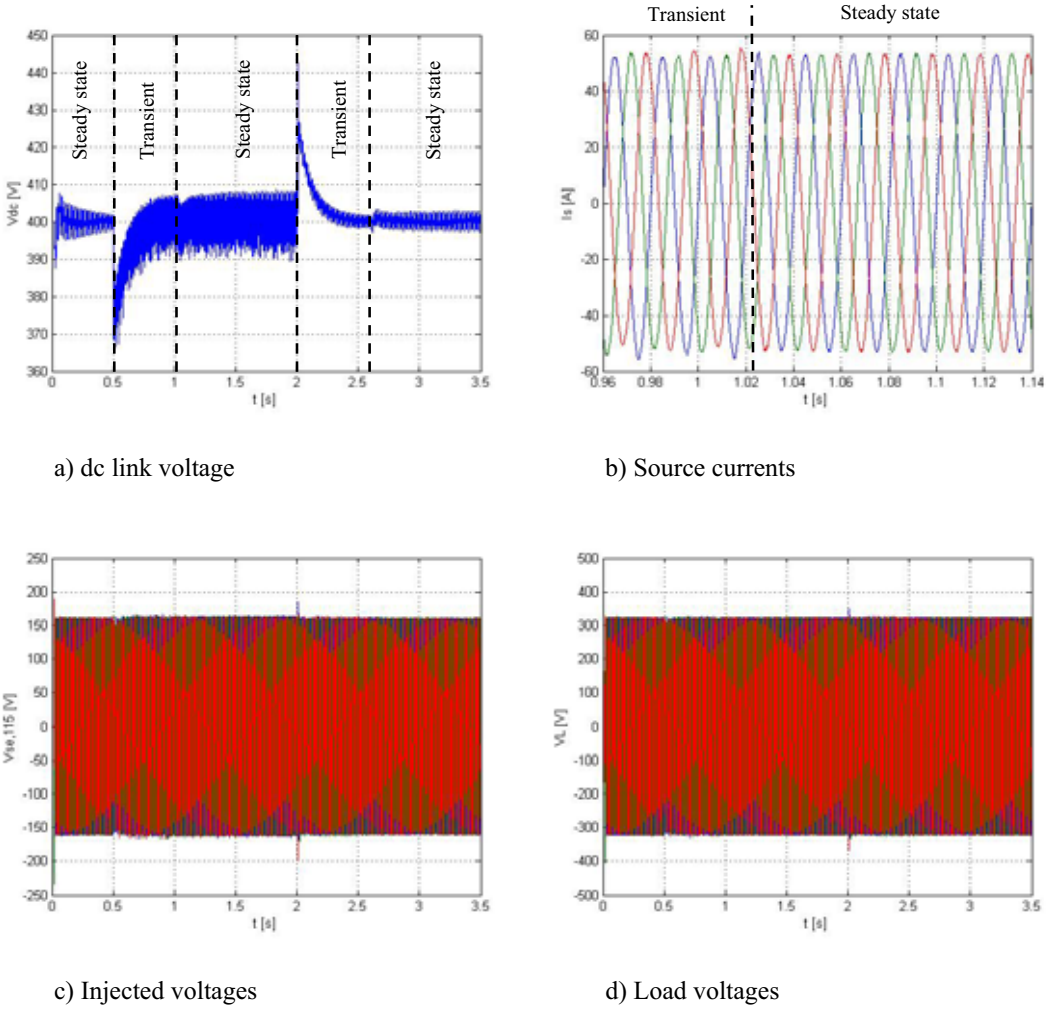
Due to the combined action of two control strategies, proposed in sections 6.2 and 6.3, the injected voltage (Fig.6.12.c) and the load voltage (Fig.6.12.d) have substantially improved. Now, both in steady state and during the transients the voltage injected by the series converter meets the requirement (162 V peak). From Fig.6.12.d we can see that the magnitude of the load voltage is constant throughout the simulation. Thus, after applying the proposed control strategies, the load voltage does not suffer from deviations during the transients.

The simulation results shown in Fig.6.12 demonstrate an evident improvement comparative with the case when none of the control strategies proposed in sections 6.2 and 6.3 is used. To make certain of this, one can compare Fig.6.2.a with Fig.6.12.a, Fig.6.3.a with Fig.6.12.c and Fig.6.4.a with Fig.6.12.d.

6.5. Summary

When a load is either connected or disconnected to/from the UPQC or a voltage sag/swell on the supply side occurs, the dc link voltage undergoes a transient, deviating from the reference. This dc link voltage deviation causes deviation in the voltage injected by the series compensator, which in turn has an effect on the load voltage. In order to

transient mode of operation and then back to steady state mode of operation took place respectively at 2.0035 s and at 2.6089 s. From Fig.6.12.a we can see that the dc link voltage deviation is less than 50 V (12.5%). Thus, the dc link capacitor voltage rating only has to be 12.5% higher than the reference dc link voltage (400 V). Also, since the dc link voltage does not drop below $0.7854 \cdot V_{dc,ref}$, there is no need the series inverter to be operated in nonlinear mode in order to output the required voltage.



a) dc link voltage

b) Source currents

c) Injected voltages

d) Load voltages

Fig.6.12. Simulation results for combined action of two control strategies

Fig.6.11 shows the supply currents when the adaptive dc link voltage controller is used. The transient period lasts from 0.5 s to 1.05 s. During this interval, the cut-off frequency of the LPF is 300 Hz and the supply currents are distorted (the magnitude varies), but this distortion only lasts for 0.55 s. At 1.05 s the controller is switched to steady-state parameters and from this point the supply currents are no longer distorted. Thus, by applying the proposed adaptive control strategy the system performance is satisfactory both in steady state and during the transients.

6.4. Simulation results for combined action of two control strategies

To obtain a better UPQC performance during both the steady state and transient conditions, those two control strategies proposed and analysed in sections 6.2 and 6.3 have been combined together and the simulation results are shown in Fig.6.12. In order to be able to compare the results, the same operation conditions as described in sections 6.2 and 6.3 have been simulated. Thus, at 0.5 s the full load was connected to UPQC and at 2 s it was disconnected. Throughout the simulation the supply voltage has a 50% sag. The supply nominal voltage is 230 V rms and the reference dc link voltage has been set to 400 V. At about 0.503 s the dc link voltage is lower than the lower threshold (485 V peak) and the dc link voltage controller is switched to transient mode of operation (cut-off frequency of LPF is 300 Hz, and $K_p^{300} = 0.6\ A/V$ and $K_i^{300} = 17.2\ A/(V \cdot rad)$ are used). Since at 1.025 s the average dc link voltage error had become lower than the threshold (0.1 V), the dc link voltage controller switched to steady state mode of operation (cut-off frequency of LPF is 50 Hz, and $K_p^{50} = 0.2\ A/V$ and $K_i^{50} = 2.8\ A/(V \cdot rad)$ are used). Similar switching to

As we can see from Fig.6.10 the maximum dc link voltage deviation is around 30 V which is 7.5% of the reference dc link voltage ($V_{dc,ref} = 400\,V$). The limit for dc link voltage deviation has been mentioned above and it is 23%. Thus, now the dc link voltage deviation is much below the limit. Comparing the results presented in Fig.6.10 and those presented in Fig.6.6.a, it can be concluded that by using the proposed adaptive controller the dc link voltage deviations during the transients have been considerably reduced (from about 50% to 7.5%).

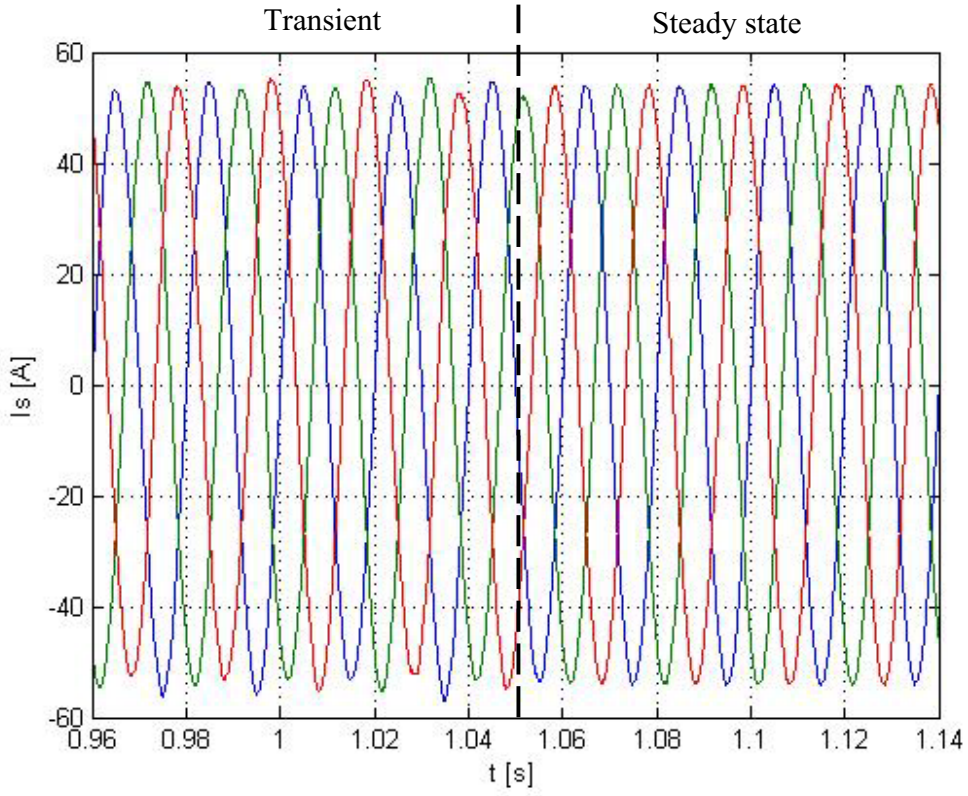


Fig.6.11. Supply currents when the adaptive dc link voltage controller is used

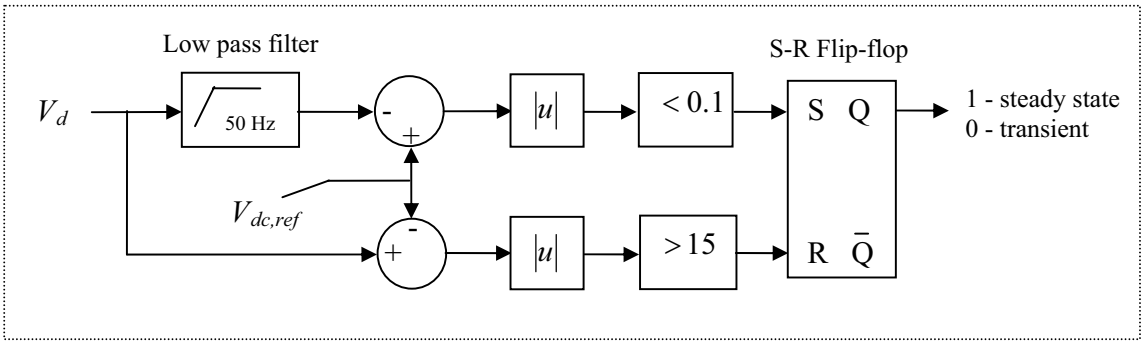


Fig.6.9. Control block for determination of the system condition

The above presented adaptive control strategy has been incorporated into the UPQC simulation model presented in section 3.4 and the simulation results are shown below. Fig.6.10 shows the dc link voltage when the adaptive dc link voltage controller is used. By connecting and disconnecting the full UPQC load while having a 50% voltage sag on supply side, the most severe disturbances have been created. At 0.5 s the full load was connected to the UPQC and at 2 s it was disconnected that caused transient dc link voltage deviations.

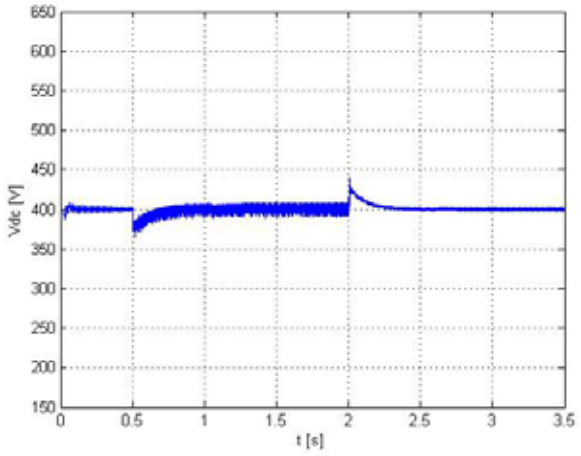


Fig.6.10. dc link voltage when the adaptive dc link voltage controller is used

used. When the transient occurs the controller switches to the LPF with 300 Hz cut-off frequency and the matching PI controller parameters $K_p^{300} = 0.6\ A/V$ and $K_i^{300} = 17.2\ A/(V \cdot rad)$ are applied. After some time, the transient disappears and the controller comes back to steady state parameters (LPF with 50 Hz cut-off frequency and K_p^{50}, K_i^{50}). Thus, the LPF cut-off frequency and the PI controller parameters are automatically adapted according to the system mode of operation. The PI controller parameters were first calculated applying the Ziegler-Nichols tuning rules [22], and then adjusted through simulations.

The starting point for the transient condition is considered to be the moment when the dc link voltage deviation gets bigger than the normal steady-state deviation. For example, for a system having $V_{dc,ref} = 400\,V$ the normal steady-state deviation can be as high as 15 V. Thus, if it appears that $\left|V_{dc} - V_{dc,ref}\right| > 15$, then the dc link voltage controller switches to transient condition parameters. The transient is considered to disappear when $\left|V_{dc,av}^{50} - V_{dc,ref}\right|$ is smaller than some threshold, which is close to zero and its value is determined by the system precision. Here, $V_{dc,av}^{50}$ is the average dc link voltage obtained at the output of the LPF with 50 Hz cut-off frequency. Fig.6.9 shows the control block for determining whether the system is in steady state or in transient condition.

distorted (the magnitude varies), whereas there is no such distortion if a LPF with 50 Hz cut-off frequency is used.

Taking into consideration the above observations, it can be concluded that using a LPF with 50 Hz cut-off frequency enables the system to have satisfactory steady state performance but slow dynamic response (large dc link voltage deviation and slow restoration), whereas using a LPF with 300 Hz cut-off frequency results in much better dynamic response but unsatisfactory steady state performance of the system. Thus, the use of a LPF with 50 Hz cut-off frequency is suitable for steady state operation, whereas during the transient operation a LPF with 300 Hz cut-off frequency is preferable. Hence, in order to have a better system performance both in steady state and during the transients an adaptive dc link voltage controller should be used. Such a controller has been developed and its diagram is shown in Fig.6.8.

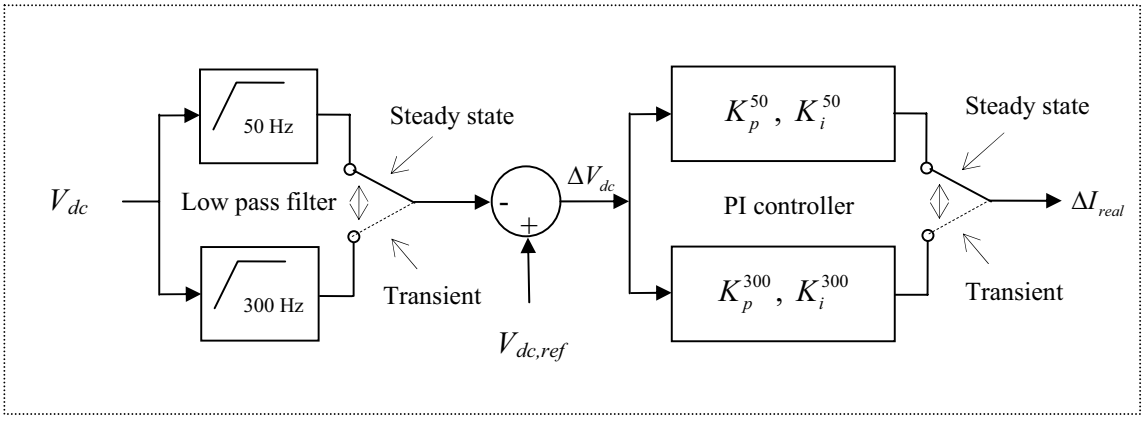
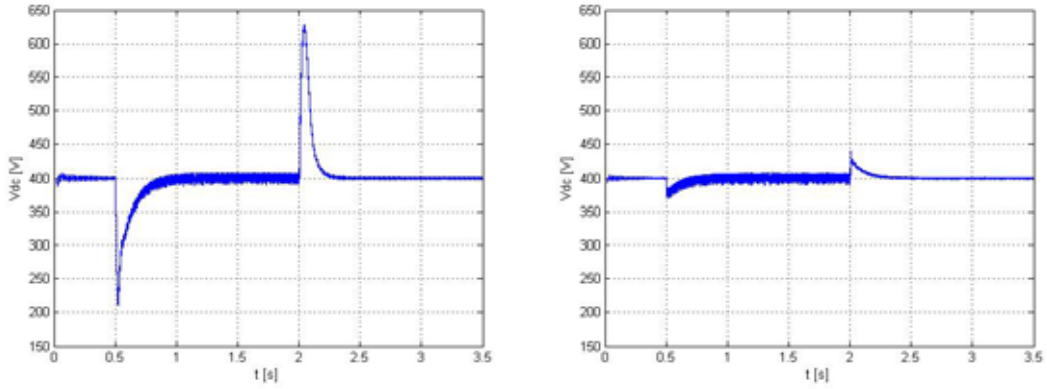


Fig.6.8. Adaptive dc link voltage controller

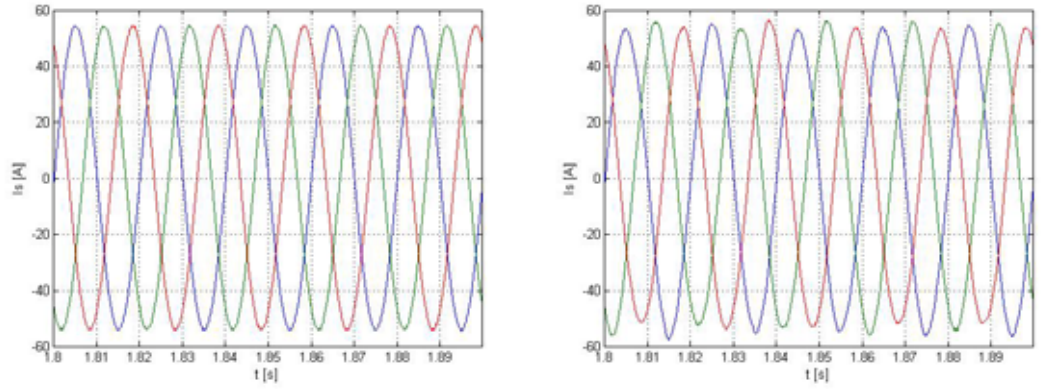
During the steady state operation, the LPF with 50 Hz cut-off frequency is active and the corresponding PI controller parameters $K_p^{50} = 0.2\ A/V$ and $K_i^{50} = 2.8\ A/(V \cdot rad)$ are

are much bigger when a LPF with 50 Hz cut-off frequency is used. Thus, using a LPF with 300 Hz cut-off frequency the dc link voltage deviation can be considerably reduced.



a) cut-off frequency is 50 Hz b) cut-off frequency is 300 Hz

Fig.6.6. dc link voltage



a) cut-off frequency is 50 Hz b) cut-off frequency is 300 Hz

Fig.6.7. Supply currents

In Fig.6.7 the steady state supply currents for the same two cases are shown. As we can see here, when using a LPF with 300 Hz cut-off frequency the supply currents are

fundamental component of the reference current, which compensates for the conduction and switching losses, thus maintaining the dc link voltage constant.

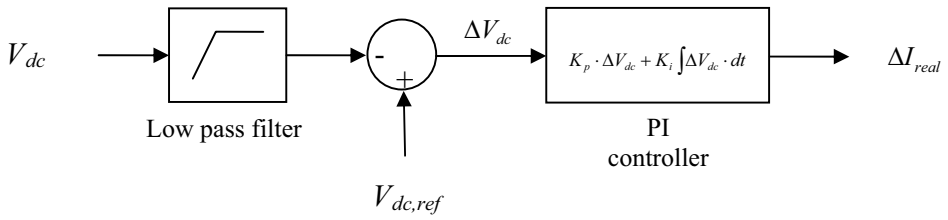


Fig.6.5. dc link voltage control block

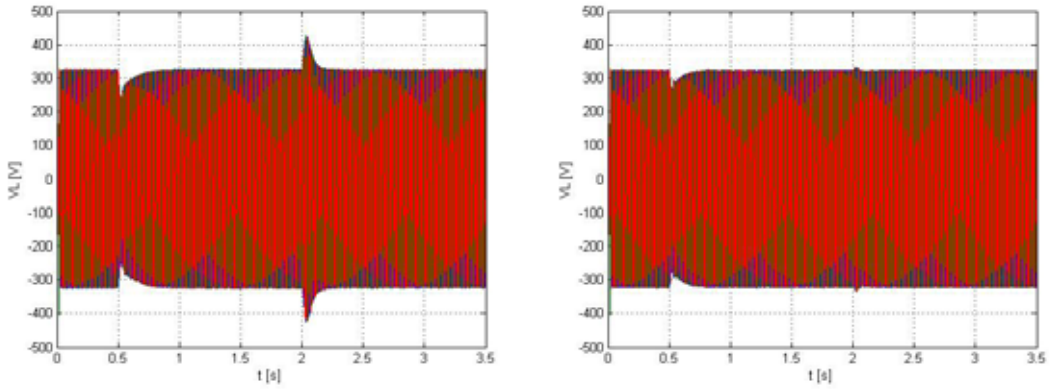
The real/reactive power injection may result in dc link voltage ripple [21]. To filter this ripple a low pass filter (LPF) is generally used (see Fig.6.5), which introduces a finite delay. The frequency of the dc link voltage ripple can be as low as 50 Hz. Thus, the cut-off frequency of the LPF should not exceed 50 Hz; otherwise, the LPF will pass the ripple and ΔI_{real} will contain the ac component that in turn will cause distortion in the supply current. On the other hand, the lower the LPF cut-off frequency, the longer the dc link voltage settling time. Also, the dc link voltage deviation is bigger.

The dc link voltage for two cases, obtained through simulation, is shown in Fig.6.6. In the first case (see Fig.6.6.a) the cut-off frequency of the LPF is 50 Hz and the PI controller parameters are: $K_p = 0.2\ A/V$ and $K_i = 2.8\ A/(V \cdot rad)$. In the second case (see Fig.6.6.b) the cut-off frequency the LPF is 300 Hz and the PI controller parameters are: $K_p = 0.6\ A/V$ and $K_i = 17.2\ A/(V \cdot rad)$. At 0.5 s the load was connected to the UPQC and at 2 s it was disconnected. This connection/disconnection of the load caused transient deviations of the dc link voltage. As we can see from Fig.6.6, the dc link voltage deviations

voltage deviation depends on the depth of the source voltage sag/swell, the size of the load connected/disconnected to/from the UPQC, the dc link capacitor rating and the performance of the dc link voltage controller. In the previous section it was concluded that the situations when $V_{dc} < 0.7854 \cdot V_{dc,ref}$ should be avoided, otherwise, the magnitude of the fundamental component of the series inverter output voltage is lower than $\frac{V_{dc,ref}}{2}$. Thus, by some means, the dc link voltage drop has to be limited to 27.32% of $V_{dc,ref}$. Also, the dc link transient overvoltages have to be limited to some reasonable value. The transient dc link voltage deviation can be reduced through proper choice of the dc link capacitor rating and design of the dc link voltage controller. Rather than increasing the dc link capacitor rating (which adds extra cost to the UPQC) a design-based solution has been derived which is presented in the following. Better performance of the dc link voltage controller is achieved by applying an adaptive control strategy.

The dc link voltage control is achieved by adjusting the small amount of real power flowing through the shunt inverter into the dc link capacitor, thus compensating for the conduction and switching losses and keeping the dc link voltage constant. This small amount of real power is adjusted by changing the amplitude of the real fundamental component of the reference current. A PI controller is normally used (since it contributes to zero steady-state error in tracking the reference) for determining the magnitude of this compensating current from the error between the average voltage across the dc capacitor and the reference dc link voltage [62]. The dc link voltage control block is shown in Fig.6.5. The output of the dc link voltage control block (ΔI_{real}) is the amplitude of the real

$V_{dc} < 0.7854 \cdot V_{dc,ref}$. In this condition, though the series converter is in square-wave mode of operation, its output voltage is lower than the requirement (162 V, peak) for full compensation of 50% supply voltage sag. Unless the dc link voltage is sufficiently increased, the series injection is lower than 162 V peak and the load voltage is lower than reference (325 V, peak). Thus, proper measures have to be taken in order to avoid the situation when $V_{dc} < 0.7854 \cdot V_{dc,ref}$. In this regard, a solution is proposed and analyzed in the following section.



a) m_a is constant

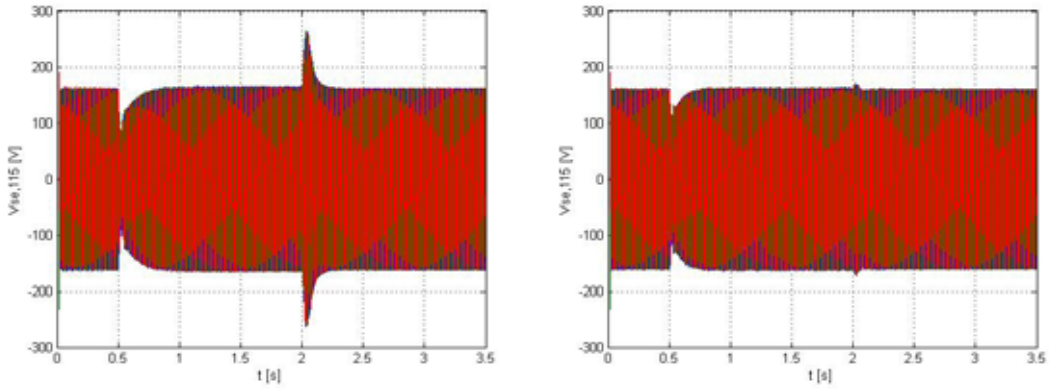
b) m_a is adjusted according to $V_{dc,act}$

Fig.6.4. Load voltages

6.3. DC link voltage control

As it was mentioned earlier in this chapter, there exist dc link voltage transients during which the average voltage across the dc link capacitor deviates from its reference value. Such transients can occur when a load is either connected or disconnected to/from the UPQC or a voltage sag/swell on the supply side takes place. The severity of the dc link

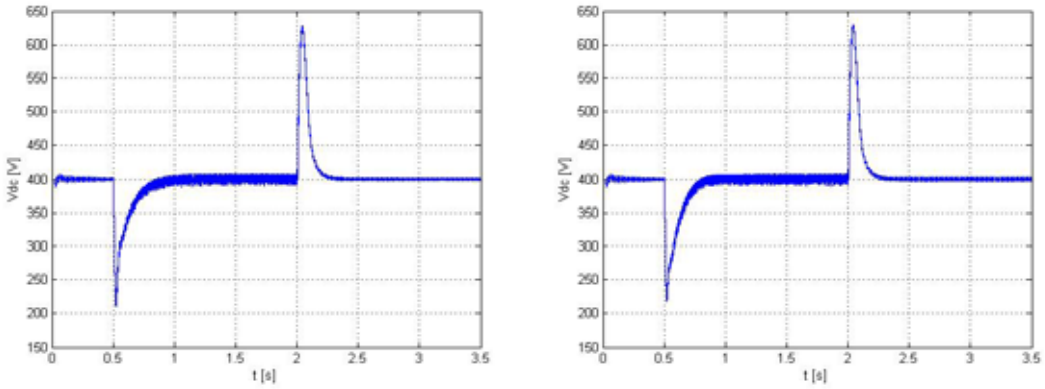
to 1 s and from 2 s to 2.4 s), due to the dc link voltage deviations and with m_a kept constant, the series converter is injecting an inappropriate voltage. In turn, this causes load voltage deviations during the transients (see Fig.6.4.a. In the first transient (from 0.5 s to 1 s) the load voltage magnitude drops down to 240 V peak (74 % of the nominal), and in the second transient (from 2 s to 2.4 s) it increases up to 425 V peak (131% of the nominal).



a) m_a is constant b) m_a is adjusted according to $V_{dc,act}$

Fig.6.3. Injected voltages

In Fig.6.3.b and Fig.6.4.b respectively, the series injected voltages and the load voltages are presented for the case when the modulation ratio m_a is continuously adjusting in accordance with $V_{dc,act}$. As we can see from these figures, during the second transient (from 2 s to 2.4 s), the voltage deviation is negligible. Thus, the overvoltage on the load side has been removed through continuous adjustment of m_a in accordance with $V_{dc,act}$. However, there is still voltage deviation during the first transient (from 0.5 s to 1 s). During this transient the dc link voltage drops below the above mentioned limit,



a) m_a is constant b) m_a is adjusted according to $V_{dc,act}$

Fig.6.2. dc link voltage

The reference dc link voltage is set to 400 V. As we can see from Fig.6.2, the connection of full load to UPQC at 0.2 s results in a deep drop (around 50%) in the dc link voltage. Due to the dc link voltage controller action, the dc link voltage is restored back to its reference value at about 1 s. The disconnection of the full UPQC load at 2 s results in a big overvoltage (around 50%) across the dc link capacitor, which is eliminated at around 2.4 s, again due to the dc link voltage controller action. As we can see from Fig.6.2, the dc link voltage dynamics in case when m_a is adjusted according to $V_{dc,act}$ looks the same as when m_a is kept constant.

In Fig.6.3, voltages injected by the series converter are shown for those two cases mentioned above. Having a 50% sag, the supply voltage is: $V_s = 0.5 \cdot 230 = 115\,V$, rms. In order to bring the load voltage to the nominal level (230 V line to neutral, rms) the series converter has to inject 162 V (peak). From Fig.6.3.a we can see that in steady state the series converter is injecting the required voltage. However, during the transients (from 0.5 s

2. The amplitude modulation ratio m_a calculated according to (6.7) is also applied if it is not greater than unity ($m_a \leq 1$) and the system is in steady state;
3. If the system is in steady state, and according to (6.7) $m_a > 1$, then m_a is made equal to the conventional amplitude modulation ratio, $m_a = m_{a,ref}$;
4. Situations when $V_{dc} < 0.7854 \cdot V_{dc,ref}$ and, as a consequence the magnitude of the fundamental component of the series inverter output voltage is lower than $\frac{V_{dc,ref}}{2}$, should be avoided. This can be achieved through proper choice of the dc link capacitor rating and design of the dc link voltage controller.

The control strategy proposed above has been investigated through simulations. The proposed control block has been incorporated into the UPQC simulation model presented in section 3.4 and the simulation results are presented in the following. The disturbances have been created by applying a 50% sag in the supply voltage and connecting the full load to the UPQC at 0.5 s and disconnecting it at 2 s. In Fig.6.2 the dc link voltage is shown for two cases. In first case (Fig.6.2.a) the modulation ratio m_a for series inverter is kept constant. In second case (Fig.6.2.b) m_a is continuously adjusted to reflect the dc link voltage variations.

the inverter output voltage in the liner modulation mode is $\hat{V}_{out(1),\max} = \frac{V_{dc,ref}}{2}$, and this corresponds to unity conventional amplitude modulation ratio ($m_{a,ref} = 1$). In steady state, the actual dc link voltage $V_{dc,act}$ is not ripple free and contains both dc and ac components. The dc component is kept constant and equal to $V_{dc,ref}$, due to dc link voltage controller. During the intervals of time when the ac component is negative, the actual dc link voltage $V_{dc,act}$ is smaller than $V_{dc,ref}$ and $\frac{V_{dc,ref}}{V_{dc,act}} > 1$. Thus, as can be seen from (6.7), when $m_{a,ref} = 1$ and $\frac{V_{dc,ref}}{V_{dc,act}} > 1$, the amplitude modulation ratio is greater than unity ($m_a > 1$). This causes the inverter to be operated in the nonlinear mode, and as a consequence, low frequency harmonics appear in the inverter output voltage. In order to avoid such situations, if in steady state the expression (6.7) results in an amplitude modulation ratio which is greater than unity, $m_a > 1$, then it should be made equal to the conventional amplitude modulation ratio, $m_a = m_{a,ref}$.

In conclusion, the following recommendations and control rules for the series inverter are derived:

1. If the dc link voltage deviates from its reference $V_{dc,ref}$ by a value greater than the maximum steady state ripple, then it is considered that the system is in transient condition and expression (6.7) is used for calculating the amplitude modulation ratio m_a;

for linear modulation mode $\frac{V_{dc,ref}}{2}$. From (6.4), it can also be concluded that the desired magnitude of the fundamental frequency component of the inverter output voltage $\hat{V}_{out(1)}$ can be obtained for dc link voltages not lower than 78.54% of the reference dc link voltage $V_{dc,ref}$. For dc link voltages below this value the magnitude of the fundamental component of the inverter output voltage is lower than $\frac{V_{dc,ref}}{2}$, which may appear to be insufficient in the case of severe supply voltage sag conditions. Thus, the situations when $V_{dc} < 0.7854 \cdot V_{dc,ref}$ should be avoided, and this can be achieved through proper selection of the dc link capacitor rating and design of the dc link voltage controller.

Expression (6.5), for calculating the amplitude modulation ratio, can be rewritten in the following way:

$$m_a = 2 \cdot \frac{\hat{V}_{out(1)}}{V_{dc,act}} \cdot \frac{V_{dc,ref}}{V_{dc,ref}} = m_{a,ref} \cdot \frac{V_{dc,ref}}{V_{dc,act}} \tag{6.7}$$

where $m_{a,ref} = 2 \cdot \frac{\hat{V}_{out(1)}}{V_{dc,ref}}$ is the amplitude modulation ratio corresponding to the reference dc link voltage $V_{dc,ref}$ (the conventional amplitude modulation ratio). Then, expression (6.3) can be rewritten in the following way:

$$\hat{V}_{control} = 2 \cdot \hat{V}_{tri} \cdot \frac{\hat{V}_{out(1)}}{V_{dc,act}} = \hat{V}_{tri} \cdot m_a = \hat{V}_{tri} \cdot m_{a,ref} \cdot \frac{V_{dc,ref}}{V_{dc,act}} \tag{6.8}$$

The series inverter of the UPQC is normally operated in the linear modulation mode and it is accordingly designed. The maximum magnitude of the fundamental component of

$$\hat{V}_{out(1)} \leq \frac{V_{dc,act}}{2} \tag{6.6}$$

With an appropriate converter design, condition (6.6) holds true for most of the possible $\hat{V}_{out(1)}$ and $V_{dc,act}$ combinations. It is only under conditions of deep supply voltage sag and significant simultaneous dc link voltage drop that (6.6) can be violated. The most severe dc link voltage drops occur during transients caused by connection to the UPQC of big loads (having the rating close to the UPQC rating) while simultaneously having a deep supply voltage sag. The duration of such dc link voltage drops depends on parameters of the system under consideration and on performance of the controller responsible for maintaining the dc link voltage. The typical duration is in the range of 5-20 fundamental cycles. During the severe dc link voltage drop, the condition (6.6) can be violated which means that the series inverter will be operating in overmodulation mode. Due to overmodulation, the series inverter output voltage will contain low frequency harmonics, and these will not be filtered by the low-pass filter, since it is designed for filtering higher frequencies (switching frequencies produced by inverter). Thus, during 5-20 fundamental cycles, the voltage injected by the series converter is distorted due to overmodulation. Instead, the magnitude of the fundamental frequency component of the injected voltage is at the desired level which, in severe condition, would not be possible without overmodulation. In severe condition, due to overmodulation, according to (6.4), the magnitude of the fundamental frequency component of the inverter output voltage $\hat{V}_{out(1)}$ can be increased by up to 27.32% (this value results from expression 6.4, $\left(\frac{4}{\pi}\frac{V_{dc,ref}}{2} - \frac{V_{dc,ref}}{2}\right)\cdot 100\% = 27.32\% \cdot \frac{V_{dc,ref}}{2}$) compared with the maximum possible value

range of $m_a \leq 1.0$, the PWM pushes the harmonics into a high-frequency range around the switching frequency and its multiples [17]. In spite of this desirable feature of a sinusoidal PWM in the linear range, one of the drawbacks is that the maximum available amplitude of the fundamental-frequency component is not as high as can be needed. To increase further the amplitude of the fundamental-frequency component in the output voltage, m_a is increased beyond 1.0, resulting in overmodulation. Overmodulation causes the inverter output voltage to contain many more harmonics in the side-bands as compared with the linear range (with $m_a \leq 1.0$). The harmonics with dominant amplitudes in the linear range may not be dominant during overmodulation. More significantly, with overmodulation, the amplitude of the fundamental-frequency component does not vary linearly with the amplitude modulation ratio m_a. For sufficiently large values of m_a, the inverter voltage waveform degenerates from a pulse-width-modulated waveform into a square wave. Thus, in the overmodulation region (with $m_a > 1.0$), the amplitude of the fundamental-frequency component of the inverter output voltage is [17, p.210, expression 8-12]:

$$\frac{V_{dc}}{2} < \hat{V}_{out(1)} < \frac{4}{\pi}\frac{V_{dc}}{2} \tag{6.4}$$

From (6.2), taking into consideration that now $V_{dc} = V_{dc,act}$, the amplitude modulation ratio is:

$$m_a = 2 \cdot \frac{\hat{V}_{out(1)}}{V_{dc,act}} \tag{6.5}$$

For keeping the amplitude modulation ratio in the linear range $m_a \leq 1.0$, the following condition must be satisfied:

link voltage $V_{dc,ref}$. This compensation technique can be easily implemented both in DSP based and analog control schemes. From (6.1) and (6.2) the magnitude of the modulating signal is:

$$\hat{V}_{control} = 2 \cdot \hat{V}_{tri} \cdot \frac{\hat{V}_{out(1)}}{V_{dc}} \tag{6.3}$$

Conventionally, when calculating the magnitude of the modulating signal, $V_{dc} = V_{dc,ref}$ is used in (6.3). Since $\hat{V}_{tri}$ and $V_{dc,ref}$ are constants, $\hat{V}_{control}$ is a function of only one variable, $\hat{V}_{out(1)}$. Thus, if the actual dc link voltage $V_{dc,act}$ deviates from its reference value $V_{dc,ref}$, this deviation has no effect on $\hat{V}_{control}$ and for a particular $\hat{V}_{out(1)}$ the magnitude of the modulating signal $\hat{V}_{control}$ is constant in both steady state and transient conditions.

In order to adjust $\hat{V}_{control}$ in accordance with the dc link voltage variation, $V_{dc} = V_{dc,act}$ has to be used in (6.3). Now $\hat{V}_{control}$ is a function of two variables: $\hat{V}_{out(1)}$ and $V_{dc,act}$. Since the calculation of $\hat{V}_{control}$ is performed continuously, any dc link voltage deviation has immediate effect on $\hat{V}_{control}$. Thus, during the transient, when the dc link voltage is undergoing a sag/swell, the magnitude of the modulating signal $\hat{V}_{control}$ is accordingly adjusted and the amplitude of the fundamental frequency series inverter output voltage $\hat{V}_{out(1)}$ remains unaffected by this disturbance. Consequently, the series compensator is able to inject the appropriate voltage, and the load side voltage magnitude is maintained at the desired level both in steady state and during the dc link voltage transients.

Normally, the amplitude modulation ratio is kept in the linear range $m_a \leq 1.0$, for which the amplitude of the fundamental-frequency voltage varies linearly with m_a. In this

$$m_a = \frac{\hat{V}_{control}}{\hat{V}_{tri}} \tag{6.1}$$

where $\hat{V}_{control}$ is the magnitude of the control signal and $\hat{V}_{tri}$ is the amplitude of the triangular signal, which is generally kept constant.

The magnitude of the fundamental frequency component of the VSI output voltage depends on both input dc voltage and amplitude modulation ratio:

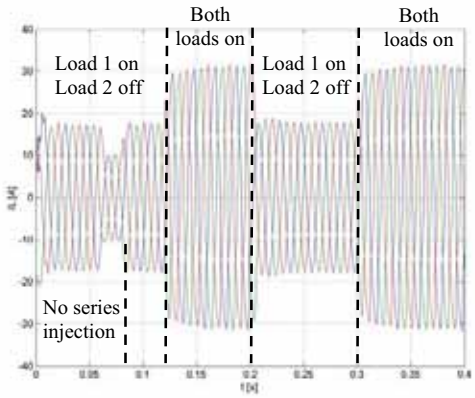
$$\hat{V}_{out(1)} = m_a \cdot \frac{V_{dc}}{2} \tag{6.2}$$

In typical applications, the inverter input dc voltage V_{dc} is usually kept constant in magnitude. Then the output ac voltage is controlled by varying the amplitude modulation ratio m_a or, to be more precise the magnitude of the control (modulating) signal $\hat{V}_{control}$. For a certain $\hat{V}_{out(1)}$ the corresponding m_a is easily calculated from (6.2) and then $\hat{V}_{control}$ is calculated from (6.1). Provided V_{dc} is constant, for $\hat{V}_{out(1)}$ to be constant for a certain time interval of interest, m_a has to be kept constant too. However, if m_a is kept constant throughout this time interval of interest, while V_{dc} is deviating from the reference (for which m_a was calculated) then $\hat{V}_{out(1)}$ will also deviate from the expected value. From (6.2), if a constant $\hat{V}_{out(1)}$ is required, while V_{dc} is deviating from the reference, m_a has to be accordingly adjusted. Thus, it is proposed that during the transient the amplitude modulation ratio m_a of the series inverter sinusoidal PWM voltage controller is continuously adjusted to match the actual dc link voltage $V_{dc,act}$ rather than the reference dc

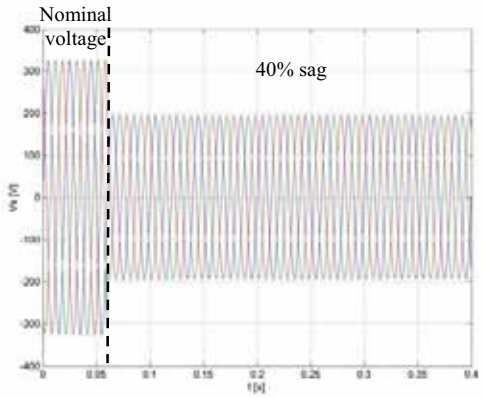
From Fig. 6.1.c we can see that the deviation of V_{dc} from its reference value can be as high as 10%. Due to this considerable dc link voltage deviation, the voltage injected by the series compensator during the interval 0.08-0.4 s has significant deviations, as is clear from Fig. 6.1.e. This variation in the injected voltage has clearly an effect on the load voltage. During the interval 0.08-0.4 s, the load voltage has noticeable magnitude variations, Fig. 6.1.d. Thus, during the transient, when the dc voltage is deviating considerably from its reference value, appropriate control action has to be taken in order for the series compensator to be able to inject the appropriate voltage. This is especially important when the supply system is undergoing a deep sag (for example 50%). Also, solutions for diminishing the dc voltage deviation during the transient must be investigated.

6.2. Control of series inverter

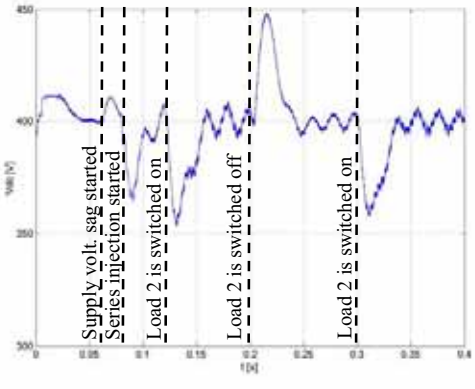
Various schemes are used to pulse-width modulate the switches of the series inverter in order to shape the output ac voltages to be as close to a sine wave as possible. Of these the sinusoidal PWM scheme discussed in detail in [17] is widely used. In this scheme the switching pulses are generated by comparing the sine waveform (control signal) with the triangular waveform (carrier signal) through an analog or digital comparator. The PWM control signal is set high when the control signal has a higher numerical value than the carrier signal and is set low when the carrier has a higher numerical value. The amplitude modulation ratio m_a is defined as:



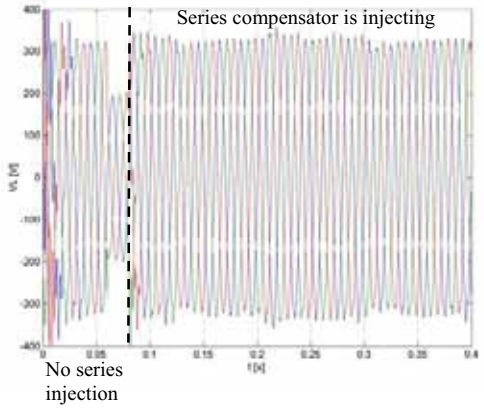
a) Load currents



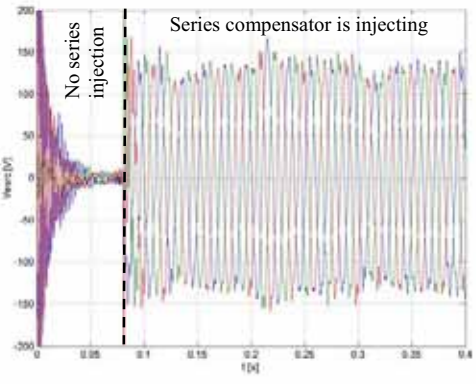
b) Source voltages



c) Voltage across the dc capacitor



d) Load voltages



e) Injected voltages

Fig. 6.1. Voltage variations due to load change

reference value at about 0.04 s, Fig. 6.1.c. Throughout the operation of the UPQC, the dc capacitor voltage is controlled to match the reference by the shunt compensator. At 0.06 s voltage sag of 40% is created, Fig. 6.1.b, and it is not removed or changed in value during the analysed period (0-0.4 s). Because of this sag and, since during the interval 0.06-0.08 s there is no series compensation, the load voltage decreased and as a consequence the load current also decreased. From Fig. 6.1.c it can be seen that during this interval (0.06-0.08 s) the dc voltage is going through a transient and its average value is deviating from the reference value (400 V). At 0.08 s the series compensator is put into operation and from this point the appropriate voltage is injected in series with the utility. As a result of this series compensation, the load voltage is restored, Fig. 6.1.d. As a consequence, the load current is also restored to its pre-sag level, Fig. 6.1.a. The dc voltage exhibits another transient during the interval 0.08-0.12 s. At 0.12 s one more load (7 kVA) is connected. Again we can see a dc voltage transient during the interval 0.12-0.16 s. At 0.2 s the second load is disconnected and this also caused the dc voltage deviation during the interval 0.2-0.24 s. At 0.3 s the second load was connected again causing a transient in the dc voltage during the interval 0.3-0.34 s.

Chapter 6

CONTROL OF UPQC DURING THE TRANSIENTS

6.1. Introduction

One significant feature of the UPQC is that typically a dc capacitor is connected between the VSIs (voltage source inverters), rather than a dc source. Because neither series nor shunt compensators are lossless, a special dc link voltage controller is required to maintain the dc capacitor average voltage at a constant level. In the UPQC, the shunt compensator is usually responsible for this voltage regulation. In the steady state, the average dc link voltage is maintained at a certain preset level, but during the transient this is not the case. Such a transient can occur when a load is either connected or disconnected to/from the UPQC or a voltage sag/swell on the supply side occurs. Since it takes a finite time interval to calculate the new reference current, the shunt compensator cannot immediately response to the load change. In addition to this, some settling time is required to stabilise the controlled parameter around its reference. Consequently, after a load changing instant there exists some transient period during which the average voltage across the dc capacitor deviates from its reference value.

Fig. 6.1 presents an example of how the dc link voltage can vary when the load changes. The shunt compensator is introduced into operation at 0.02 s and at that instant a 8.5 kVA load is connected. The dc capacitor reference voltage is 400 V, and due to the appropriate control actions the voltage across the dc capacitor is stabilised around this

both through simulations and experiments that if the "not filtered" supply current $i_s^{/}$ is tracked, rather than the supply current after filtering i_s, stability is maintained using the hysteresis controller.

Simulation results show an evident reduction of both supply currents and load voltages distortions, achieved by connecting filter capacitors in parallel with the load and applying the proposed control approach.

As an alternative to hysteresis band controller it was proposed to operate the shunt active filter in voltage control mode. In voltage control mode the current injected by shunt active filter is controlled indirectly by controlling the voltage generated by the shunt inverter. The appropriate control block has been derived and the effectiveness of this approach has been proved through simulations. Using this control approach the switching frequency of the shunt inverter is kept constant which is not possible in hysteresis band controller. Thus, the preference should be given to the voltage control mode strategy rather than the hysteresis control technique. Further work should involve the implementation of the proposed voltage control mode strategy in the laboratory prototype UPQC and experimental validation of the results obtained so far through simulations.

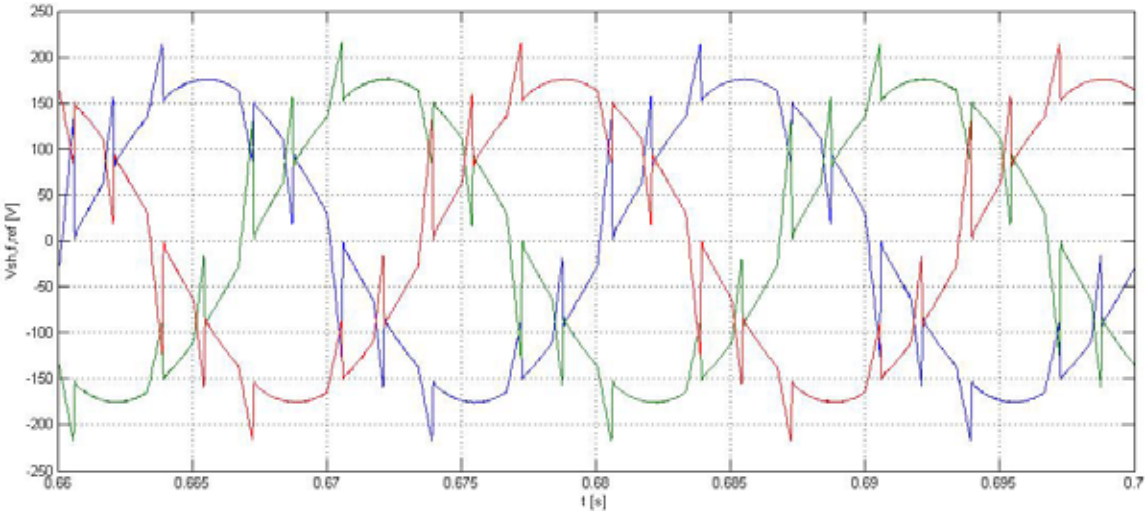
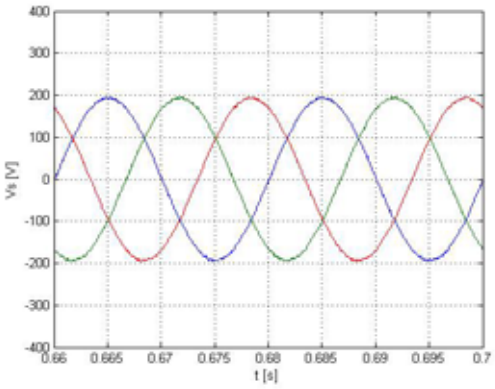


Fig.5.19. Shunt inverter reference voltages

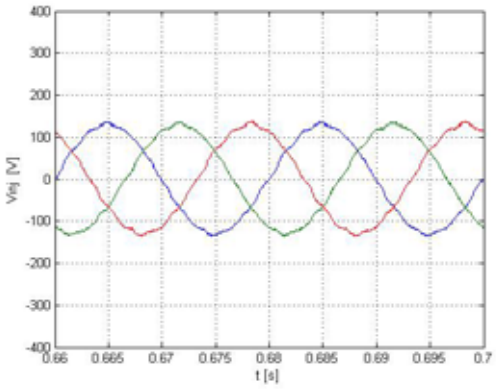
5.4. Summary

If a UPQC is connected to a weak supply point, the load side voltage can become unacceptably distorted due to the switching frequencies in the supply current. In order to prevent the switching frequencies generated by the shunt inverter entering into the grid, the LC or/and LCL filters are used for interfacing the shunt VSI with the distribution network. However, the incorporation of a second or higher order filter involves more complex control techniques to maintain the system stability.

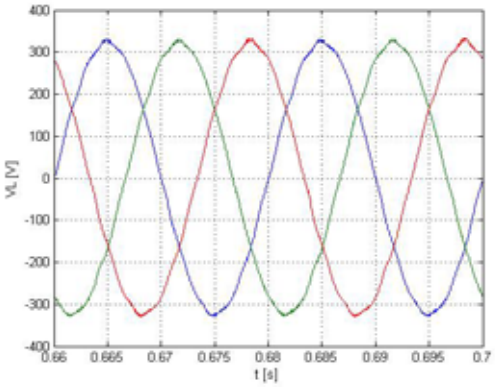
Because of its simplicity, the hysteresis based control strategy is very attractive from the practical implementation point of view. In this chapter, a control approach for avoiding the stability problem while using the hysteresis control technique is proposed with application to the shunt component of the UPQC incorporating an LCL filter. It is shown



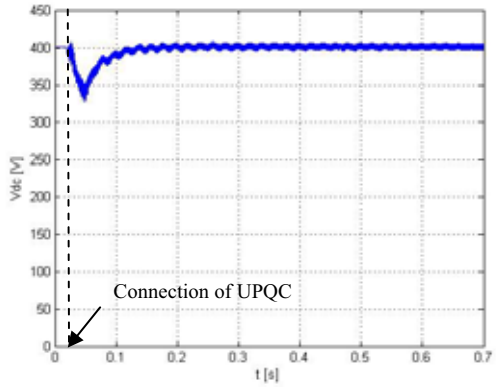
a) supply voltages (THD=0.85%)



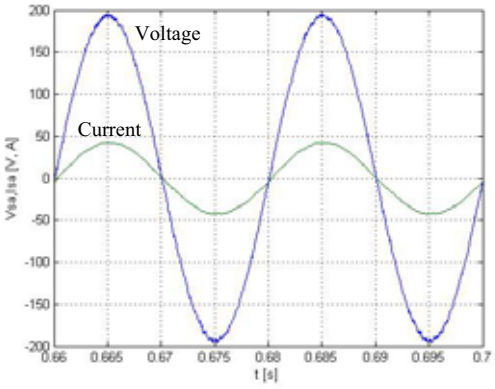
b) voltages injected by series active filter



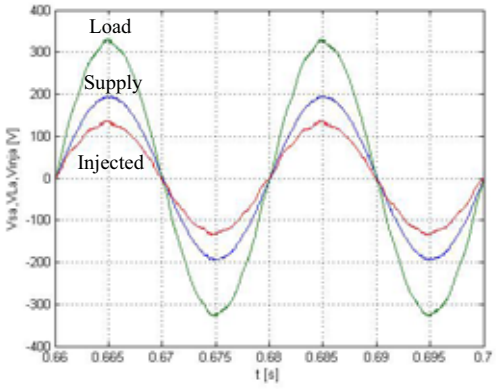
c) load voltages (THD=1.42%)



d) dc link voltage



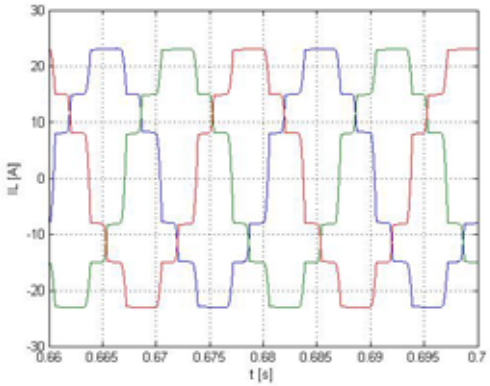
e) supply voltage and current, phase a



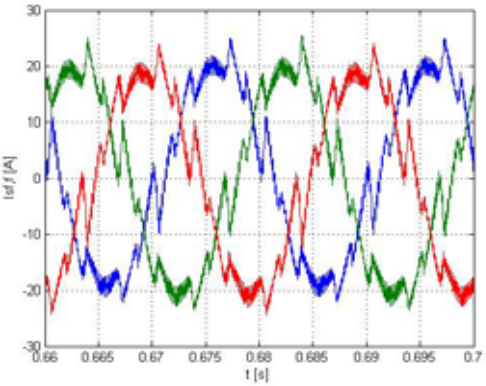
f) supply, injected and load voltages, phase a

Fig.5.18. Simulation results: voltages

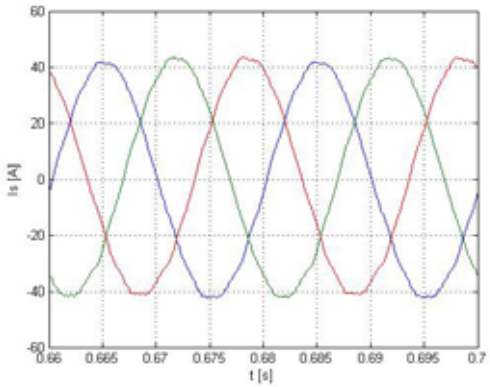
Fig.5.18.f) we can see that the supply, injected and load voltages are in phase. In Fig.5.19 the shunt inverter reference voltages are shown.



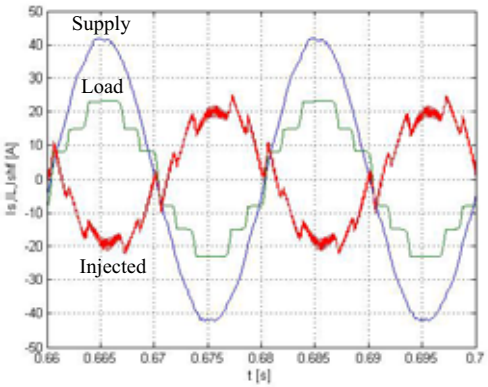
a) load currents (THD=14.18%)



b) currents injected by shunt active filter



c) supply currents (THD=2.25%)



d) supply, load and injected currents, phase a

Fig.5.17. Simulation results: currents

5.3.2. Simulation results

A three-phase three-wire UPQC with the same power circuit parameters as described in section 3.4 is investigated. The simulation model is created in Simulink and the UPQC is connected at 0.02 s. The series inverter is controlled to compensate for sags/swells in the supply voltage. The shunt inverter is controlled to compensate for unbalance, reactive and harmonic components of the load current and to maintain the average voltage across the DC capacitor at the level of 400 V. The shunt inverter is controlled in voltage control mode applying the strategy presented above. The shunt and series inverters switching frequencies are respectively 6 and 10 kHz.

The supply voltages are balanced and undistorted, but suffering from a 40% sag. In order to compensate for voltage sag, the series compensator is injecting voltage in phase with the supply current.

The simulation results are presented in Fig.5.17 – Fig.5.19. In Fig.5.17.a) the load currents are shown. Fig.5.17.b) shows the currents injected by the shunt active filter. From Fig.5.17.c) we can see that the supply currents are balanced sinusoids which fulfill the 8% restriction established by IEEE Standard 519-1992. In Fig.5.17.d) the load, supply and injected currents of phase *a* are shown together. From Fig.5.18.e), it can be seen that the supply current is in phase with the supply voltage. Both supply and load voltages, shown respectively in Fig.5.18.a) and Fig.5.18.c), are much below the 5% limit recommended by IEEE Standard 519-1992. The load voltages are kept at the nominal level, 230 V rms (325 V peak, see Fig.5.18.c)), and the dc link voltage is kept at 400 V (see Fig.5.18.d)). From

be used in expression (5.2). Thus, the load voltage v_L is measured and passed through a Fourier filter for fundamental extraction. Then, the resulting load voltage fundamental $v_{L(1)}$ is used in (5.2), instead of v_L.

Considering the simplifications and assumptions presented above, the expressions (5.1) and (5.2) are transformed into the following formulae for calculating the shunt active filter reference current $i_{f,ref}$ and the corresponding shunt inverter reference voltage $v_{f,ref}$:

$$i_{f,ref} = i_L^{/} - i_{s,ref} - i_{c(1)} \tag{5.3}$$

$$v_{f,ref} = v_{L(1)} + R \cdot i_{f,ref} + L\frac{di_{f,ref}}{dt} \tag{5.4}$$

Based on expressions (5.3) and (5.4), the control block for voltage-source voltage-controlled shunt inverter has been derived, as shown in Fig.5.16.

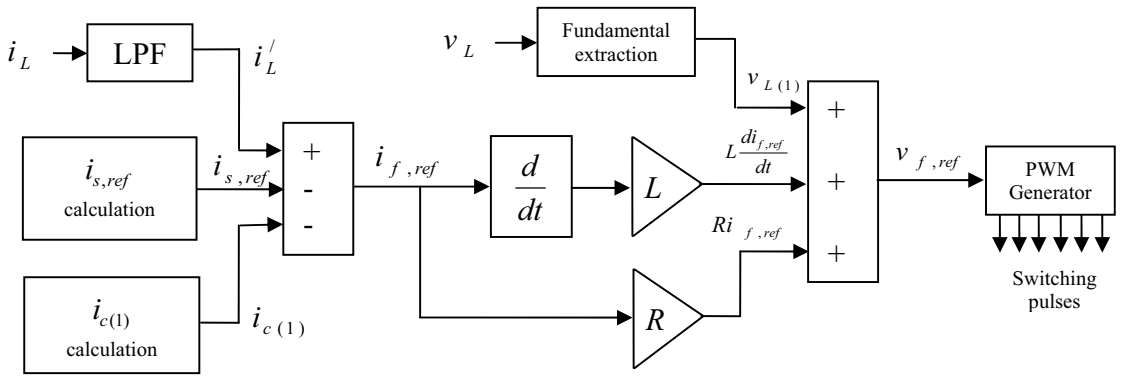


Fig.5.16. Shunt inverter voltage control block

where:

R - lumped resistance of shunt filtering inductor and shunt coupling transformer;

L - lumped inductance of shunt filtering inductor and shunt coupling transformer;

v_L - load voltage;

i_L - load current;

i_s - supply current;

i_c - current injected by shunt filtering capacitor.

The load current i_L has to be measured and passed through a LPF for high frequency noise filtering. Let the resultant load current be denoted as $i_L^{/}$. Thus, in expression (5.1), i_L should be replaced by $i_L^{/}$.

If the shunt active filter is properly controlled, the supply current i_s should track the reference $i_{s,ref}$, which can be determined as explained in section 6.3, Fig.6.5, or by applying other relevant techniques. Taking this into consideration, the supply current i_s can be replaced in (5.1) by its reference $i_{s,ref}$.

Since the harmonic currents injected by shunt filtering capacitor are very small in comparison with the fundamental component, they can be neglected. Thus, the shunt filtering capacitor fundamental current $i_{c(1)}$ can be used in (5.1) instead of i_c. The calculation of $i_{c(1)}$ is a simple procedure explained in subsection 5.2.1.

If the series active filter is properly controlled, the load voltage v_L should be sinusoidal. However, in reality it contains some ripple that has to be removed before v_L can

of the shunt inverter is kept constant. This control approach with application to the force-commutated three-phase controlled rectifiers is presented in [62, pp.228-232]. The application of the same control approach to the shunt active filter is investigated below.

The equivalent circuit of shunt active filter shown in Fig.5.15 is used for deriving the formulae for calculating the shunt inverter reference current $i_{f,ref}$ and voltage $v_{f,ref}$. The shunt inverter is presented here as an ac voltage source (v_f).

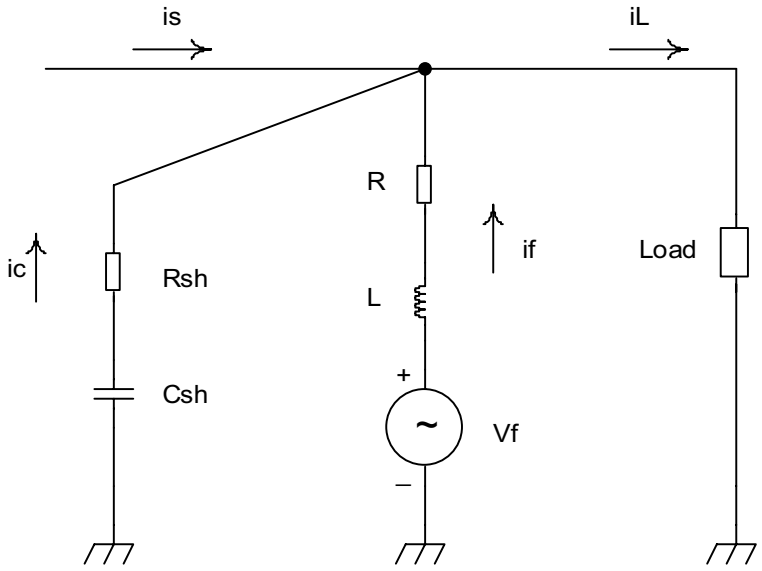


Fig.5.15. Equivalent circuit of shunt converter

Applying the Kirchhoff current and voltage laws to the circuit presented in Fig.5.15, the current injected by the shunt active filter i_f, and the corresponding shunt inverter voltage v_f are determined as follows:

$$i_f = i_L - i_s - i_c \tag{5.1}$$

$$v_f = v_L + R \cdot i_f + L\frac{di_f}{dt} \tag{5.2}$$

5.3. Operation of shunt active filter in voltage control mode

As mentioned earlier in this chapter, the implementation of hysteresis current controller is simple. Unfortunately, there are several drawbacks associated with the technique itself [62, p.382]:

1. The switching frequency cannot be predicted as in carrier-based modulators and therefore the harmonic content of the supply currents and voltages becomes random. This could be a disadvantage when designing the filtering components;
2. As in three-phase three-wire systems there is no neutral connection, the supply currents add up to zero. This means that only two currents can be controlled independently at any given instant. Therefore, one of the hysteresis controllers is redundant at a given time.
3. Although the supply currents add up to zero, the controllers cannot ensure that all the supply currents feature a zero dc component in one fundamental cycle.

5.3.1. Voltage control mode strategy

In voltage control mode the current injected by the shunt active filter is controlled indirectly by controlling the voltage generated by the shunt inverter. First the shunt active filter reference current is determined, and then the reference voltage for the shunt inverter is calculated. Knowing the shunt inverter reference voltage, the switching pulses are generated with the most well known PWM method (discussed in detail in [17]), which compares the reference signal with a triangular carrier signal. Thus the switching frequency

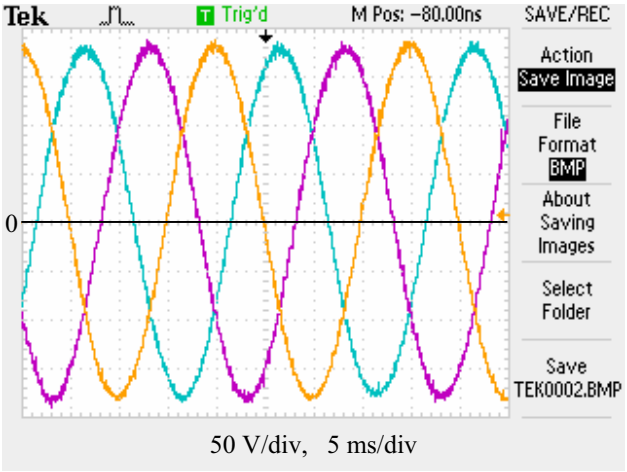


Fig.5.13. Load voltages (THD=1.23%)

In Fig.5.14 the supply voltage and current of phase *a* are shown together. From this picture it can be seen that the supply current is in phase with the supply voltage which means that the reactive component of the load current is fully compensated by UPQC.

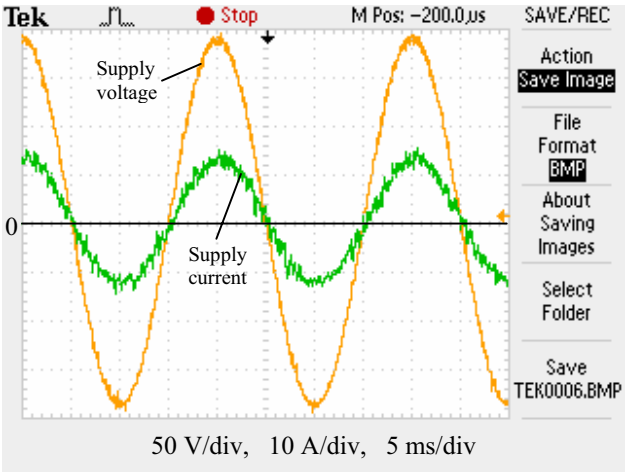


Fig.5.14. Supply voltage and current of phase *a*

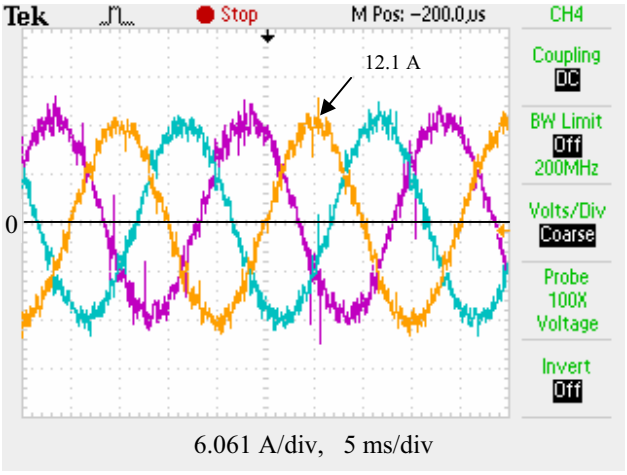


Fig.5.11. Supply currents i_s (THD=6%)

The supply and load voltages are shown in Fig.5.12 and Fig.5.13, respectively. Both the supply and load voltage THDs are below the 5% limit recommended by IEEE Standard 519-1992.

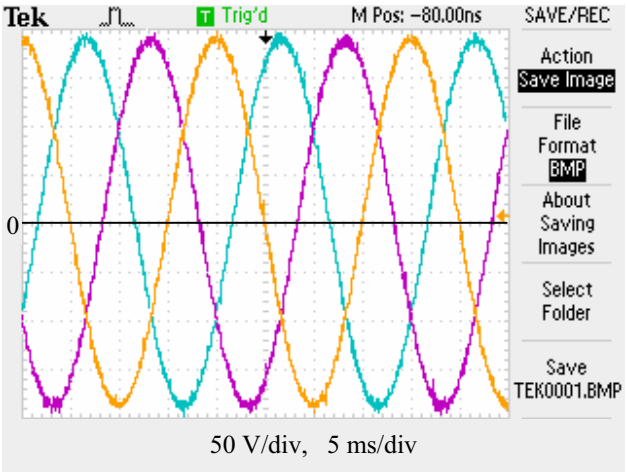


Fig.5.12. Supply voltages (THD=0.87%)

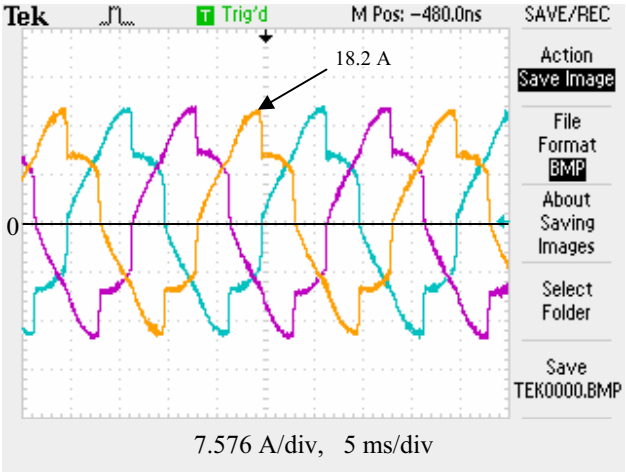


Fig.5.9. Load currents (THD=16.88%)

In Fig.5.10 the "not filtered" supply currents i_s' are shown. As expected, these currents contain switching frequency ripple. Due to the shunt connected filtering capacitor Csh a good portion of this switching frequency ripple is cancelled. Fig.5.11 shows the "filtered" supply currents i_s (after filtering out the switching frequency ripple). The supply current i_s THD is 6%, whereas the limit according to IEEE Standard 519-1992 is 8%.

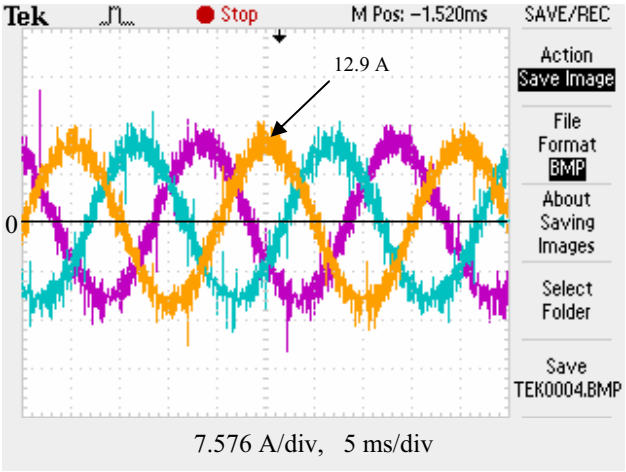


Fig.5.10. Supply currents i_s' (THD=7.2%)

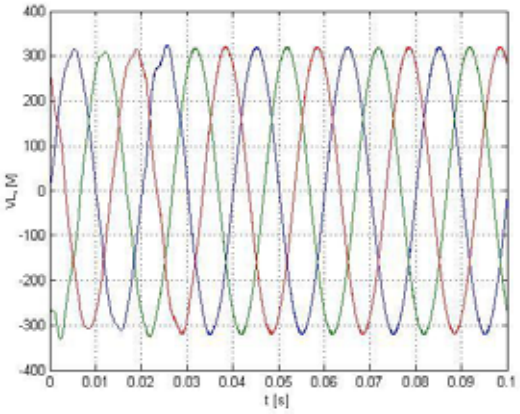


Fig.5.8. Load voltages when a filter capacitor is connected in parallel with the load and $i_s^{/}$ is tracked using hysteresis control (THD=0.5%)

5.2.3. Experimental results

The experimental results have been obtained with the laboratory prototype UPQC presented in Chapter 3. Three loads were connected to UPQC: 1) a resistive load; 2) an inductive load; and 3) a nonlinear load. The nonlinear load was composed of a power resistor connected to a three-phase rectifier. The total load current is presented in Fig.5.9 (THD=16.88%). The supply voltages were balanced, free of distortion and at the nominal level (230 V rms, line to line). An ac power source produced by California Instruments has been used throughout the experiment, providing quasi-ideal 50 Hz sinusoidal voltage. The hysteresis controller for shunt inverter has been implemented in TI320F2812 fixed point DSP. The "not filtered" supply current $i_s^{/}$ was used as the feedback variable. The measurements have been performed using a Tektronix oscilloscope, type TPS 2024.

by simply comparing the voltage waveforms from Fig.5.3 and Fig.5.8. The voltages from Fig.5.8 appear to contain no ripple.

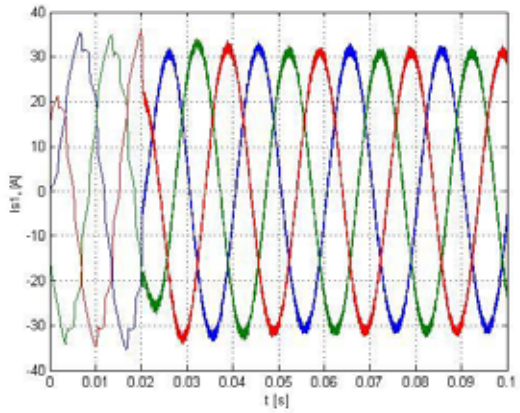


Fig.5.6. Supply currents $i_s^{/}$ when a filter capacitor is connected in parallel with the load and $i_s^{/}$ is tracked using hysteresis control (THD=3.2%)

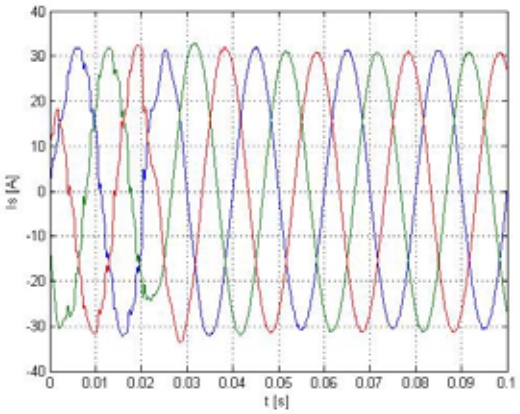


Fig.5.7. Supply currents i_s when a filter capacitor is connected in parallel with the load and $i_s^{/}$ is tracked using hysteresis control (THD=1%)

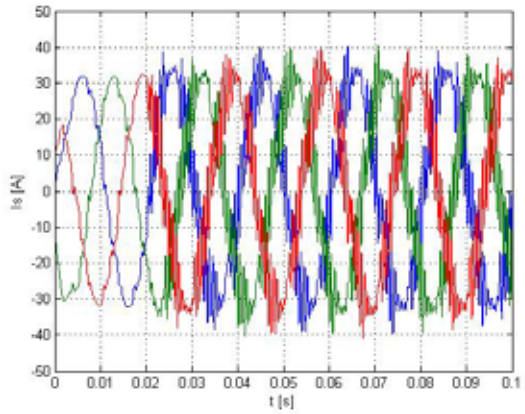


Fig.5.4. Supply currents i_s when a filter capacitor is connected in parallel with the load and i_s is tracked using hysteresis control (THD=18%)

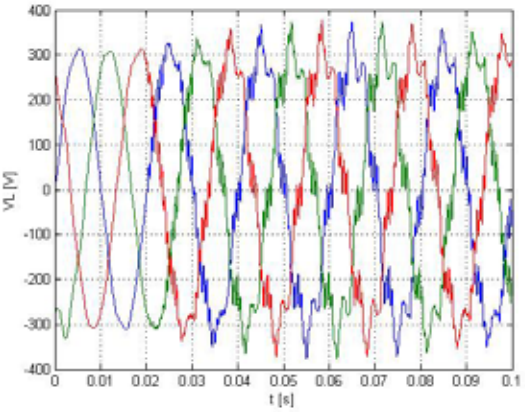


Fig.5.5. Load voltages when a filter capacitor is connected in parallel with the load and i_s is tracked using hysteresis control (THD=16%)

In order to make the system stable, $i_s^{/}$ was used as the feedback variable. The tracked currents $i_s^{/}$ are shown in Fig.5.6. These currents, like those in Fig.5.2, contain switching frequency ripple. However, the supply currents i_s (Fig.5.7) appear free of switching frequency harmonics, which have been diverted to the filter capacitors Csh (see Fig.5.1). Now, the supply current i_s THD is 1%. As a result, there is significant improvement in load voltage THD, as shown in Fig.5.8 (THD=0.5%). This improvement is easy to observe

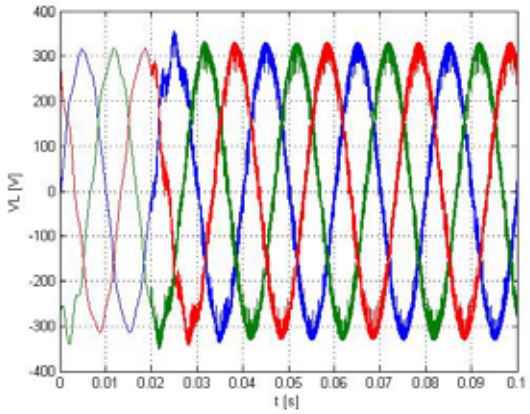


Fig.5.3. Load voltages when there is no filter capacitor in parallel with the load (THD=7.2%)

In Fig.5.4 and Fig.5.5, the supply currents and load voltages are shown respectively for the case when a filter capacitor is connected in parallel with the load and i_s is tracked. As it can be seen from these results, the supply currents become highly distorted (THD=18%) as do the load voltages (THD=16%), whereas better results than those presented in Fig.5.2 and Fig.5.3 were expected after introducing the filter capacitors. A hysteresis band on i_s fails to keep the current within the limits resulting in unacceptable distortion of both supply current and load voltage. Thus, the system is unstable in this case and i_s can not be used as the feedback variable, to get the desired performance of power quality.

interfaced with the grid, only through inductor. The supply currents are sinusoids containing some acceptable switching frequency ripple. The total harmonic distortion (THD) is 3.2%, which is much lower than the limit value established by IEEE 519 standard (8% for the system under consideration). Although the supply current THD is within the limits prescribed by the above mentioned standard, the load side voltage contains unacceptable ripple. Fig.5.3 shows the load side voltages. It is conspicuous that the load voltages become unacceptably distorted after the UPQC is introduced into operation at 0.02 s. In this particular case the load voltage THD is 7.2%, whereas according to above mentioned standard it should not exceed 5% for 69 kV and below. Thus a filter capacitor should be connected in parallel with the load in order to get rid of the switching frequency ripple from the supply currents and, as a result, from the load voltages.

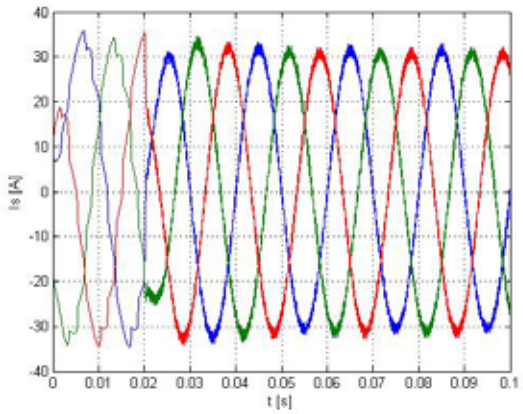


Fig.5.2. Supply currents when there is no filter capacitor in parallel with the load (THD=3.2%)

Properly tuned filter capacitor Csh cancels the switching harmonic currents, but it also injects some amount of the fundamental frequency reactive current. In order to compensate for this reactive current the inverter should additionally generate the reactive current of the same magnitude but the opposite polarity. Since the voltage across the filter capacitor V_L and its capacitance C_{sh} are known, the magnitude of this current is easily determined: $\hat{I}_c = \omega C_{sh} \hat{V}_L$ ($\hat{V}_L$ is the load voltage magnitude). Thus, in addition to the component which is in phase with the supply voltage, the reference feedback current $i'_{s,ref}$ will contain a small reactive component.

The filter capacitor C_{sh} value should be selected in such a way that the resonance with the feeder inductance at the fundamental frequency is excluded. Recommendations on proper capacitor selection in this respect are given in [3]. Also, resonance at switching frequencies is possible if proper design is not applied. The resonance at switching frequencies can be avoided by proper choice of switching frequency (hysteresis band) and introducing of a small value damping resistor R_{sh} in series with the filter capacitor C_{sh} (see Fig.5.1).

5.2.2. Simulation results

A three-phase three-wire UPQC has been investigated using the simulation model described in section 3.4, and the simulation results are presented in the following. The UPQC is connected at 0.02 s. In Fig.5.2 the supply currents are shown for the case when there is no filter capacitor connected in parallel with the load and the shunt VSI is

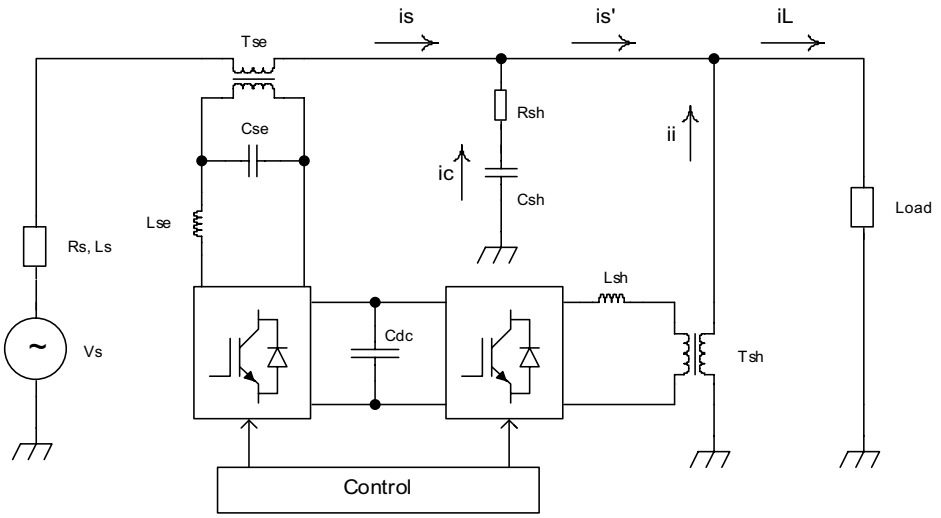


Fig.5.1. Diagram of system under consideration

The reference supply current is compared with the actual supply current and the error is passed through a hysteresis controller, which is explained in detail in [3,62]. The hysteresis control strategy has the advantage of simple practical implementation; that is why it is so attractive and preferable in many cases.

As mentioned above, in order to prevent the switching frequencies generated by the shunt inverter entering into the grid, an LC/LCL filter is used for interfacing the shunt VSI with the distribution network. In order to divert the switching harmonic currents, a filter capacitor Csh (see Fig.5.1) is connected in parallel with the load in each phase. If the supply current i_s (see Fig.5.1) is chosen as the feedback variable, the hysteresis controller will fail to maintain the system stability [3,73]. However, if the "not filtered" supply current $i_s^{/}$ is chosen as the feedback variable, the system is stable using the hysteresis controller. Thus, in order to assure the system stability, the hysteresis controller is tracking the "not filtered" supply current $i_s^{/}$.

In this section a control approach for avoiding the stability problem while using the hysteresis control technique is proposed with application to the shunt component of the UPQC incorporating an LCL filter. It is shown that if the output inverter current is tracked, rather than the current into the grid after the filter capacitor, stability is maintained using the hysteresis controller. Therefore, the control goal (keeping the grid current and load voltage THDs within the limits prescribed by standards) is achieved using a hysteresis controller, which is simple to implement.

The shunt inverter is controlled in such a way that the supply current is sinusoidal and in phase with the supply voltage. The "not filtered" (containing switching harmonics) supply current $i_s^{/}$ (see Fig.5.1) is used as the feedback variable. Since the waveform and phase of the supply current are known, only its magnitude needs to be determined to get the reference feedback variable. The magnitude of the reference supply current is determined using the control approach proposed in [20]. The average DC capacitor voltage is compared with the reference value and the voltage error is processed by a proportional integral (PI) controller. The average DC capacitor voltage is maintained constant and the output of the PI controller is the magnitude of the reference supply current. By properly changing the magnitude of the supply current, the average DC capacitor voltage is maintained constant. Applying this concept the control circuit can be simplified and the number of current sensors reduced.

implementation of this control technique is only possible using a DSP. The design and practical implementation of an LQR controller is not a trivial task.

Simple control strategies (for example hysteresis band control), which are reliable with first order systems, are usually unstable when applied to the second and higher order systems. Thus, in the case when an LCL filter is used for interfacing the shunt VSI with the grid, the hysteresis current controller fails to track the reference if the current injected into the distribution grid is tracked [3]. An analysis of control stability when using the third order filter is presented in [73]. It has been shown that using the current injected into the grid as the feedback variable in the control circuit, results in unstable operation of the power circuit. Instead, if the inverter output current is used as the feedback control variable the operation is stable. Thus, the hysteresis current control technique can be applied in the second and higher order systems without having stability problems if the feedback control variable is the inverter output current.

5.2. Operation of shunt active filter in current control mode

5.2.1. Hysteresis band current controller

Because of its simplicity, the hysteresis based control strategy is very attractive from the practical implementation point of view. The hysteresis band controller requires an operational amplifier (op-amp) operating in the hysteresis mode, thus the controller and modulator are combined in one unit [62].

Chapter 5

UPQC CONNECTED TO A WEAK SUPPLY POINT

5.1. Introduction

The shunt component of a UPQC uses a VSI (voltage source inverter), which is typically connected to the grid through an interface inductor. This inductor reduces the switching harmonics injected by the shunt VSI into the distribution network. However, if the UPQC is connected to a weak supply point (a weak supply system is defined as a system having appreciable internal inductance), the load side voltage and the voltage at the point of common coupling (PCC) can become unacceptably distorted due to the switching frequencies in the supply current. The level of distortion depends on the Thevenin equivalent inductance of the supply system and of the series compensator.

In order to prevent the switching frequencies generated by the shunt inverter entering into the grid, in the literature [3,60,73,74], it is proposed to use LC or/and LCL filters for interfacing the shunt VSI with the distribution network. This significantly reduces the switching frequencies in the supply current and as a consequence improves the THDs of the load and PCC voltages, bringing them to an acceptable level. However, the incorporation of a second or higher order filter involves more complex control techniques to maintain the system stability. For example in [60], it is proposed to use a Linear Quadratic Regulator (LQR), which involves extensive computation. Since the full state feedback control system is used, the reference values for all the state variables must be continuously calculated. The

from the series inverter. The overvoltage protection crowbar consists of a pair of antiparallel connected thyristors governed by a very simple Zener diode based control circuit, which does not require separate power source. In addition an overcurrent detector is used to disable the inverters in overcurrent conditions.

The effectiveness of the proposed protection scheme has been confirmed through simulations carried out in Simulink for different fault and system conditions. It has been shown that using the proposed protection scheme the series inverter is fully protected from both overcurrent and overvoltage, and the overall reliability of the equipment is enhanced. Also, an experimental overvoltage protection circuit has been designed, built, tested and incorporated into the UPQC laboratory prototype. The experimental results demonstrate the effectiveness of the proposed protection scheme once again.

protection crowbar is limited to a value slightly higher than 300 V. The thyristors are triggered into the on state after overvoltage occurrence, thus putting the voltage across the protection crowbar to zero.

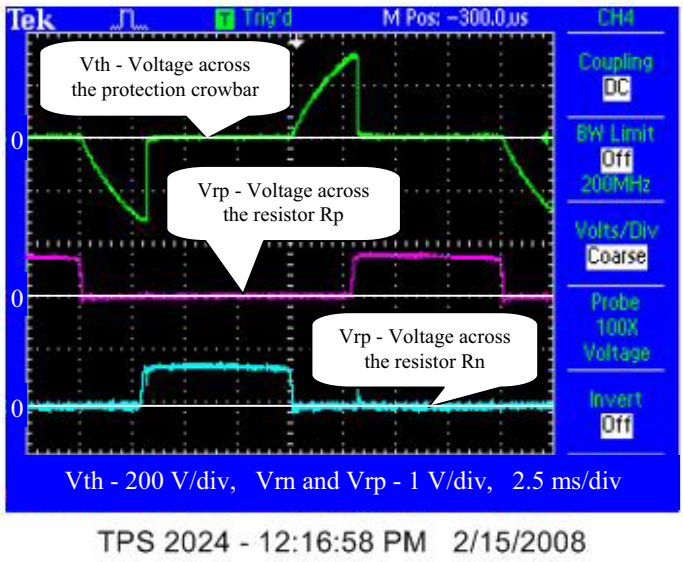


Fig.4.16. Test 4, Vs=250 V (354 V peak)

4.6. Summary

In this chapter a protection scheme for UPQC series inverter has been presented and analyzed. The proposed scheme protects the series inverter from overcurrents and overvoltages, which appear during a short circuit on load side of UPQC. The main protection element is a type of crowbar, which is connected across the secondary of the series transformer. As soon as an overvoltage appears the crowbar short-circuits the secondary of the transformer, thus removing the overvoltage and diverting the fault current

applied across the crowbar becomes higher than the threshold and the thyristors are triggered into the on state. Thus, after 4.3 ms, the protection crowbar appears as a short circuit and the voltage across it is almost zero. From Fig.4.15 we can see that the voltage across the protection crowbar is clamped to about ±300 V.

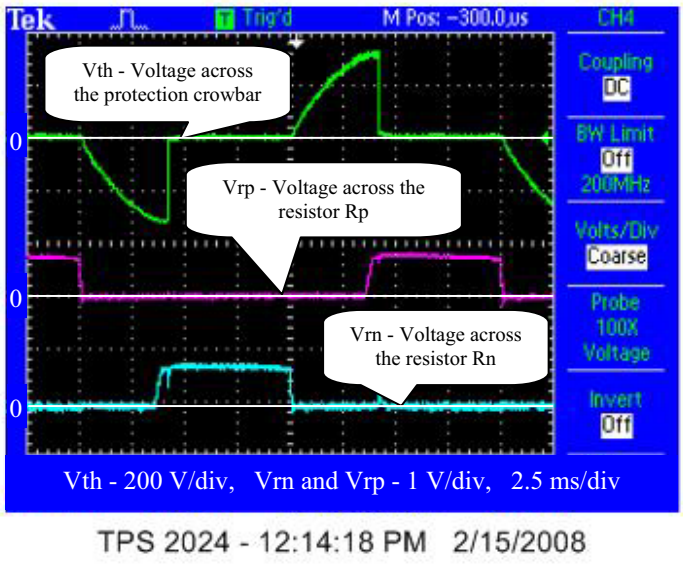


Fig.4.15. Test 3, Vs=227 V (321 V peak)

In Test 4 (see Fig.4.16), the source voltage is 354 V peak. Now, since the source voltage is greater than in Test 3, the voltage across the crowbar exceeds the threshold even faster. From Fig.4.16 we can see that the thyristors are triggered into the on state at about 3.2 ms (in Test 3 it happened at 4.3 ms). Like in Test 3, the voltage across the protection crowbar is clamped to about ±300 V.

Thus, from the above tests, it can be concluded that the protection crowbar successfully limits the voltage across it. Voltages below the threshold (300 V) appear across the crowbar without any change. In the case of overvoltage, the voltage across the

In Test 2 (see Fig.4.14), the source voltage is increased to 314 V peak. The biggest part of this voltage (slightly above 300 V) drops across the protection crowbar and the rest of it drops across that 70 Ω power resistor mentioned above (connected in series with the crowbar for limiting the source current). Since the peak voltage across the protection crowbar is now slightly higher than the threshold, voltage impulses (the magnitude is around 0.6 V) appears across the gate-cathode of thyristors (see purple and blue signals on Fig.4.14), but they are not big enough to trigger the thyristors. Thus, the thyristors are still in the off state.

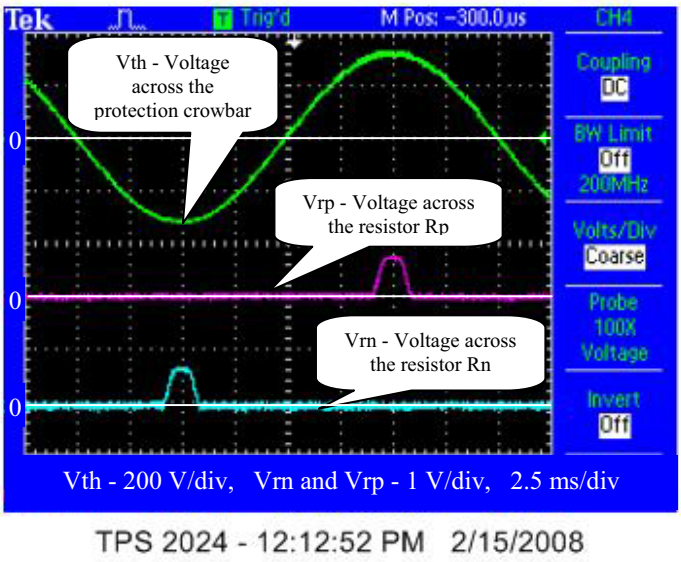


Fig.4.14. Test 2, Vs=222 V (314 V peak)

In Test 3 (see Fig.4.15), the source voltage is further increased to 321 V peak. Now, when the voltage across the crowbar is higher than the threshold, the gate-cathode voltage pulses are big enough to trigger the thyristors into the on state. At about 4.3 ms, the voltage

top signal is the voltage across the protection crowbar. The middle and bottom signals are the voltages across the resistors Rp and Rn respectively (see Fig.4.3). These are also the gate-cathode voltages of respectively positive half-cycle and negative half-cycle thyristors (THp and THn on Fig.4.3).

In Test 1, the source voltage has been set to 298 V peak, which is lower than the threshold (300 V). The results corresponding to Test 1 are shown in Fig.4.13. As we can see from this figure, the entire source voltage appears across the protection crowbar, and the gate-cathode voltages of thyristors are around zero. As expected, since the voltage across the protection crowbar is lower than the threshold, the thyristors are in the off-state and the crowbar appears as an open circuit.

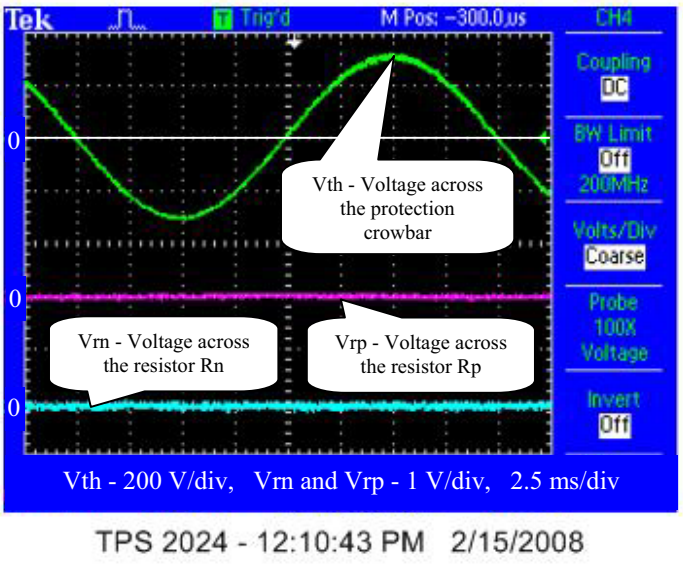


Fig.4.13. Test 1, Vs=211 V (298 V peak)

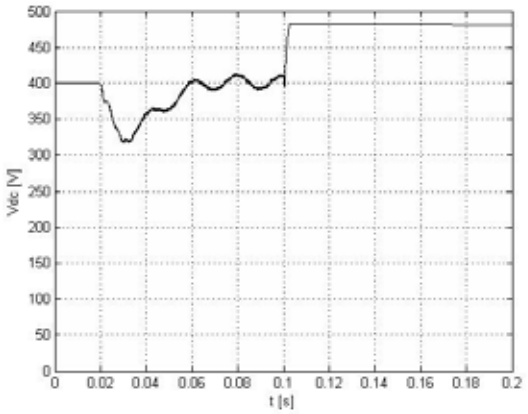


Fig.4.12. Voltage across the DC capacitor, Case Study 4

4.5. Experimental results

Based on the investigations presented above, an experimental overvoltage protection circuit has been designed, built, tested and incorporated into the UPQC laboratory prototype. The circuit diagram, PCB layout and a photograph of the overvoltage protection card are presented in Appendix E. Four Zener diodes (the breakdown voltage of each is 75 V) have been connected in series to set the protection threshold to 300 V. The protection circuit has been tasted by applying across it a range of voltage levels, close to the threshold, (i.e. below and above). A California Instruments AC Power Source has been used throughout the experiment, providing quasi-ideal 50 Hz sinusoidal voltage. In order to limit the source current, a 70 Ω power resistor has been connected in series with the protection crowbar. The measurements have been performed using a Tektronix oscilloscope, type TPS 2024. Fig.4.13 through Fig.4.16 show the experimental results for four different tests. The

steady state voltage across the secondary of the series transformer is about 180 V peak. Since the secondary voltage is less than the threshold (300 V), the overvoltage protection crowbar does not short-circuit the secondary of the transformer, and in such circumstances there is no necessity. The overcurrent through the switches of the series VSI is prevented by disabling them.

Although during the fault there is no overvoltage across the secondary of the series transformer, in a short time after the fault occurrence, the DC link voltage increased to about 480 V (see Fig.4.12). This DC link voltage increase is due to the fact that the voltage across the secondary of the transformer does not become steady immediately after the fault occurrence but goes through a transient (see Fig.4.11). During this transient, although the voltage across the secondary does not exceed 300 V (the threshold), the line-to-line voltage, which is applied through the series VSI across the DC capacitor, in the worst case can appear to be as high as 600 V. Since after the transient the DC capacitor does not discharge significantly, the voltage across it remains at the level it reached during the transient (see Fig.4.12). Therefore, the series VSI and DC capacitor ratings have to be chosen accordingly.

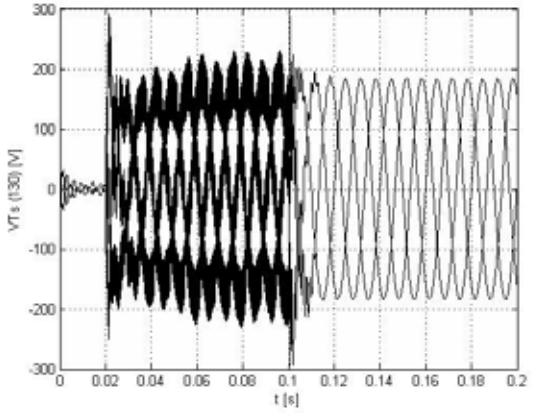


Fig.4.11. Voltages across the secondary of the series transformers, Case Study 4

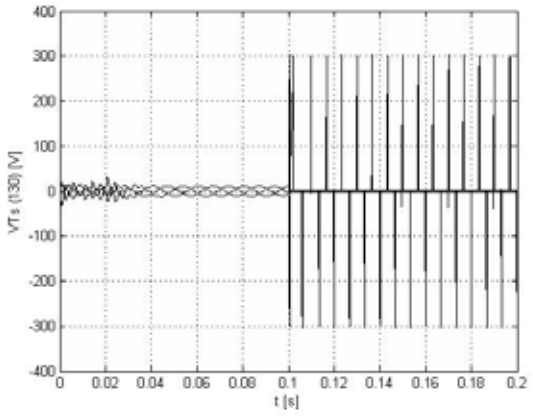


Fig.4.9. Voltages across the secondary of the series transformers, Case Study 3

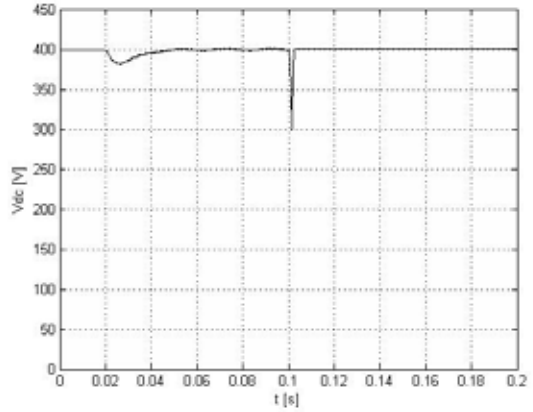


Fig.4.10. Voltage across the DC capacitor, Case Study 3

Case Study 4

As mentioned above, in the Case Study 4 the supply system is undergoing a 50% voltage sag. The supply voltage in this case is about 115 V (r.m.s.), and during the fault the voltage across the primary of the series transformer does not exceed the rating (115 V). Thus, due to such a deep voltage sag, there is no overvoltage across the secondary of the series transformer during the fault. From Fig.4.11 we can see that during the fault the

Case Study 3

In the Case Studies 3 and 4 the proposed protection is connected and the effects of its operation can be observed on the results presented below. From Fig.4.8 we can see that, after the fault occurrence (at 0.1 s), as soon as the magnitude of the current through the series VSI increased to 100 A, the protection disabled the inverter switches and the current quickly reduced to zero.

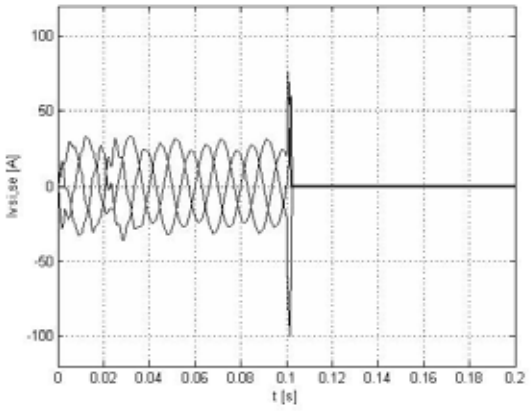


Fig.4.8. Currents through the series VSI, Case Study 3

From Fig.4.9 we can see that, due to the operation of the protection crowbar, the voltage across the secondary of the series transformer is clamped to 300 V. As a result, there is no overvoltage across the DC link (see Fig.4.10). Thus, during the fault, due to the operation of the protection, the series VSI does not experience either overcurrent or overvoltage.

Case Study 2

In the Case Study 2 there is also no protection crowbar across the secondary of the series transformer, but the series VSI is disabled during the fault. In this case, since the series VSI is disabled the current flowing through it during the fault is reduced to zero. However, an overvoltage appears across the secondary of the series transformer and, as a result, across the DC link. From Fig.4.7 we can see that the voltage across the DC capacitor is higher than 650 V. Under the present situation it exceeds the voltage limit of the DC capacitor, which will be damaged due to uncontrolled excess charge accumulation. Also, the maximum rating for the collector-emitter voltage of the series VSI IGBT switches is 600 V. Thus, the simulation results from Case Studies 1 and 2 prove that during a short circuit on the load side of UPQC the series VSI is exposed to either an overcurrent or overvoltage. In order to prevent the device being damaged a special fast acting protection has to be used.

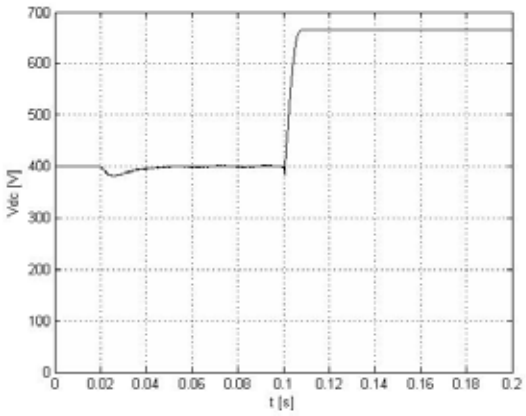


Fig.4.7. Voltage across the DC capacitor, Case Study 2

a three-phase short circuit on the load side was created at 0.1 s, which lasted for 100 ms. For the Case Studies 1, 2 and 3, the supply voltage is at the nominal level (230 V line-to-neutral), and the series compensator does not inject any voltage. In Case Study 4 the supply system is undergoing a 50% voltage sag and therefore, in order to maintain the load voltage at the nominal level, the series compensator is injecting an appropriate voltage in series.

Case Study 1

In the Case study 1 there is no protection crowbar across the secondary of the series transformer and during the fault the series VSI is not disabled. Since in this case the secondary of the series transformer is short-circuited through the series VSI switches, there is no overvoltage across it during the fault. However, as it can be seen from Fig.4.6, the series VSI experiences an overcurrent. During the fault the current through the series VSI switches exceeds 400 A (peak), whereas its maximum rating is 150 A. It is expected that the devices of the series inverter will be damaged or destroyed due to such excess current.

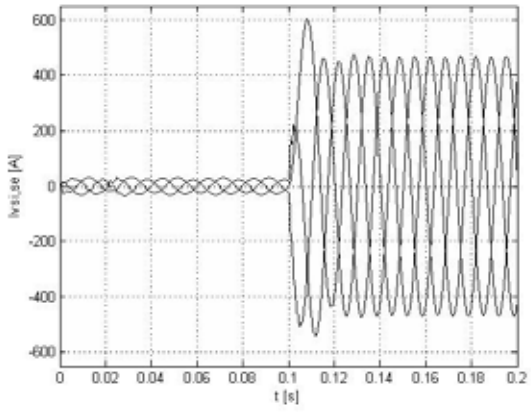


Fig.4.6. Currents through the series VSI, Case Study 1

flowing from the supply is greatly reduced which can adversely affect the upstream protection. Another, more reasonable solution is to connect the capacitor Cf across the primary of the transformer (instead of being connected across the secondary), as shown in Fig.4.3. In this case, the capacitor Cf is distant from the protection crowbar and during the short circuit the capacitor discharging does not create spikes in current through it, as shown in Fig.4.5.b) (simulation results).

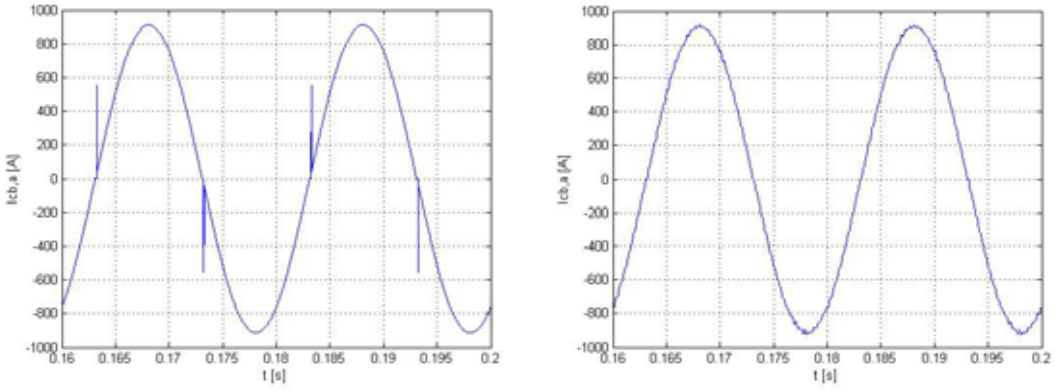
The protection scheme must not operate in case of the slight transient overvoltages that can appear across the secondary of the series coupling transformer during the normal operation of the UPQC. The erroneous tripping of the protection crowbar during the normal operation can cause a stability problem. In this case, the UPQC, instead of improving the power quality, will worsen it. In order to prevent the overvoltage protection malfunction, the reference voltage of the protection crowbar has to be set higher than the transient overvoltages which arise during normal operation. At the same time, the voltage ratings of the series VSI and DC capacitor should be chosen such that these devices can withstand the normal operational overvoltages.

4.4. Simulation results

In order to investigate the performance of the proposed protection scheme, its model was incorporated into the UPQC simulation model presented in section 3.4, and the appropriate short circuit conditions have been simulated.

The threshold for the overvoltage protection crowbar is set to 300 V. The series VSI is disabled as soon as the current through it exceeds 100 A. In all cases under investigation

secondary of the transformer, the capacitor Cf also becomes short-circuited. The current through the conducting thyristor is the sum of two components: short-circuit current originating from the supply and the series VSI; and the current due to the discharging of the capacitor Cf. The current component due to the discharging of the capacitor Cf introduces spikes in the overall short circuit current trough the protection crowbar, as shown in Fig.4.5.a) (simulation results). These spikes are periodic (once per half cycle) and put additional stress on thyristors during the discharging of capacitor Cf.



a) Cf is connected across the secondary of the series transformer

b) Cf is connected across the primary of the series transformer

Fig.4.5. Current through phase a of the protection crowbar during the short circuit

An eventual solution to this problem would be the insertion of an appropriate value resistance in series with Cf or with the protection crowbar. This can reduce the Cf discharging current and change its dynamics such that the spikes disappear. However, this solution requires additional hardware and causes additional losses. Also, if the resistor is connected in series with the protection crowbar, the magnitude of the short circuit current

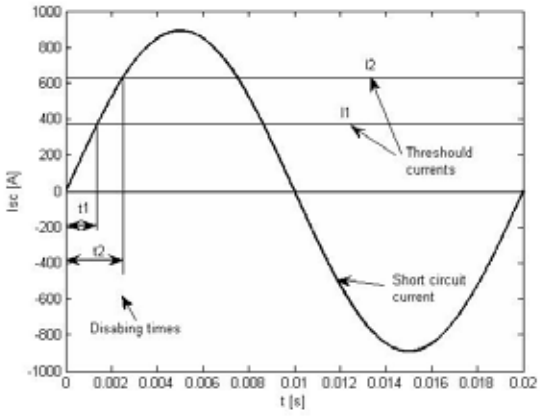


Fig.4.4. Dependence between the threshold current and disabling time

The overcurrent detector is such constructed that it continues to generate the disabling signal even after the input signal is greatly reduced or removed. In other words it memorises the overcurrent occurrence. The necessity of having the memorising action is dictated by the fact that as soon as the VSIs are disabled the currents through them are reduced to almost zero. In the absence of a memorising action the overcurrent detector would intermittently enable and disable the VSIs as long as the overcurrent condition exists. Specific reset action is required (manual or from a dedicated circuit) to reset the overcurrent detector.

In order to cancel the switching frequency harmonics produced by the series VSI, a low-pass-filter (LPF) is inserted between the series VSI and series transformer, which consists of an inductor and a capacitor. This filtering capacitor can be either connected across the secondary of the series transformer or across the primary. In Fig.4.3, the eventual connection of the filtering capacitor Cf across the secondary of the series transformer is shown by a dashed line. In this case, when the protection scheme short-circuits the

As mentioned above, the short circuit current flowing from the supply side is diverted to the thyristors of the protection scheme. However, since the series VSI remains in operation, a large current will flow through it, which comes from the DC side. In order to interrupt the path for this current, the series VSI switches have to be disabled. Thus, as soon as the secondary of the series transformer is short-circuited by the protection scheme, the gate signals of the series VSI have to be disabled in a reasonably short time. Also, in order to prevent the short circuit on the load side being fed from the DC link, through the shunt part of UPQC, the gate signals of the shunt inverter also have to be disabled. For generating the gate disabling signal a current transformer or transducer (CT) is used for measuring the current through the series VSI (see Fig.4.3). In the secondary of this current transformer an overcurrent detector is connected. During the normal operation the currents flowing through the series VSI are below the threshold value and the overcurrent detector generates an output signal, which enables the operation of both series and shunt inverter. As soon as a current higher than the threshold value is flowing through the series VSI, the overcurrent detector generates a disabling output signal, which is applied to both series and shunt VSIs gate drive circuits. The faster the overcurrent detector circuit initiates the disabling of the VSIs the better. For smaller threshold currents the disabling occurs faster (see Fig.4.4). Thus, for faster disabling of VSIs, it is preferable to have a threshold current not much higher than the maximum current through the series VSI during the normal operation.

The proposed protection scheme is a controlled crowbar, which is connected across the secondary of the series transformer and short-circuits it when an overvoltage occurs across the transformer secondary. Since a short circuit on the load side of UPQC usually results in an overvoltage across the secondary of the series transformer, the protection operates and the large short circuit current flowing from the supply side is diverted from the series inverter switches to the thyristors of the protection scheme. The inverter switches are simultaneously protected from both overvoltage and overcurrent during such a fault. The operating principle of the scheme is explained for the positive half cycle of the voltage waveform (thyristor THp is forward biased). From Fig.4.3 we can see that the voltage across the thyristors is also the same as the voltage applied to their control circuits. While the voltage across the thyristor THp is of forward polarity, but not greater than the rated breakdown voltage of the Zener diode ZDp, the latter is not conducting and the voltage across the resistor Rp is of a very low value, which is insufficient to turn-on the thyristor. Therefore, the thyristor stays forward-blocked. As soon as the forward polarity voltage across the thyristor is higher than the rated breakdown voltage of Zener diode ZDp, the latter starts to conduct and the voltage across the resistor Rp increases until it is at a sufficient level to fire the thyristor. The thyristor THp turns on and short-circuits the secondary of the transformer. When the current through the thyristor tries to go negative it turns off. During the negative half-cycle of the voltage waveform thyristor THn works on the same principle. The Zener diode breakdown voltage determines the reference voltage (at which the thyristors are triggered into on state) of the protection scheme. The diodes Dp and Dn prevent the forward conduction of Zener diodes ZDp and ZDn respectively.

4.3. Protection circuit

A protection scheme against the load side short circuits has been derived and implemented in the UPQC laboratory prototype. As mentioned earlier, if a short circuit occurs at the load side of the UPQC, the secondary of the series transformer has to be short circuited in a reasonably short time (microseconds), in order to protect the series inverter from overvoltage and overcurrent. It is proposed to accomplish this short-circuiting by using a pair of antiparallel connected thyristors, governed by a very simple Zener diode based control circuit. The proposed protection scheme is shown in Fig.4.3.

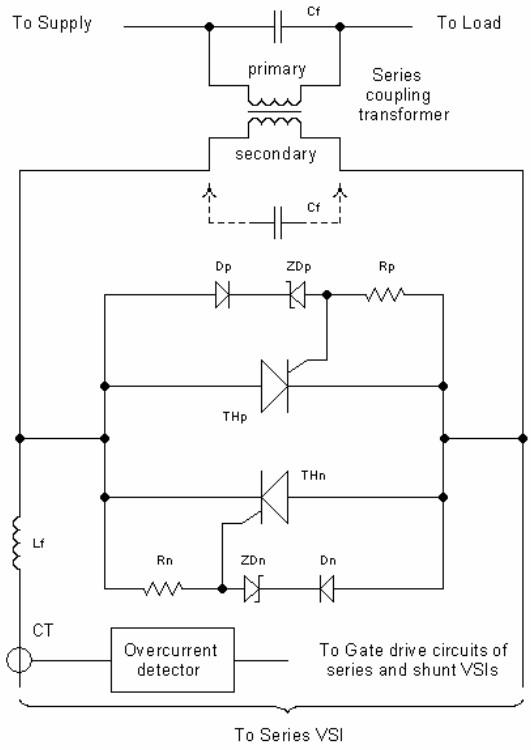


Fig.4.3. Thyristor-based series VSI protection scheme

The series VSI can not be protected from the short circuit currents by simply disabling the VSI gate signals or using circuit breakers or fuses. Circuit breakers and fuses cannot act fast enough, therefore they cannot be used for protection of power electronic devices against overcurrent. Opening the secondary of the series coupling transformer will result in failure to balance the mmf from the primary winding, which in turn will cause the transformer to be driven into excessive magnetic saturation, and an excessive voltage will appear across the secondary winding. Rather, during a short circuit on the load side, a special path must be provided for the flow of the secondary current, which will divert the excessive current from the series VSI switches. The elements forming this path are appropriately rated depending on the level and duration of the fault current to be passed trough them.

The series VSI protection must not interfere with the protection installed upstream in the distribution network. The protection systems of many pieces of power equipment, in order to clear the fault, rely on detection of substantial overcurrent. If this overcurrent is greatly reduced due to the operation of the series VSI protection, the protection installed upstream in the distribution network may not clear the fault or clear it with an unacceptably long delay. Thus, when designing the series VSI protection, such interference should be excluded.

When the supply system is undergoing a deep voltage sag, the supply voltage may appear to be not higher than the voltage rating of the series transformer primary winding. The series VSI is not experiencing overvoltage in this case. If at the same time a short circuit occurs at the load side, although the short circuit current is reduced due to the voltage sag, it is still much higher than the series VSI rating. In this case, the protection circuit must disable the inverter switches, in order to protect the series VSI from overcurrent.

The series coupling transformer is connected in series with the feeder and must be operated like a current transformer, which means that its secondary circuit has to be always closed. In normal operation, the series VSI switches provide the path for the flow of the secondary current. However, during a short circuit on the load side, the current flowing through the secondary of the series coupling transformer and hence through the series VSI switches is well above their ratings. Although the series coupling transformer is designed to withstand the short circuit current until the fault is cleared by the system protection, the series VSI switches can be destroyed if proper protection measures are not taken. In the event of a fault in a distribution network, the fault is cleared after a duration, which is determined by the time delay imposed by the protection system. This delay in turn is determined by the response time of the switching devices and the requirements of the protection co-ordination. As noted in [55-56], the total clearing time of a low-voltage circuit breaker depends on the amplitude of the fault current, but usually has a minimum value higher than 45 ms, whilst the minimum clearing time can exceed 100 ms for medium-voltage applications. The devices inside the series VSI are not able to carry the fault current for such a long duration.

scheme proposed in this chapter is simple and easy to implement, and it does not interfere with the upstream protection installed in the power distribution system. It serves to protect the series VSI from both overvoltages and overcurrents during load side short circuits.

4.2. Protection issues for series inverter

Before proceeding to explain the operation of the proposed protection scheme it is worth highlighting the issues involved with a load side short circuit. When a load side short circuit occurs, the voltage across the load is nearly zero, and almost all the supply voltage becomes proportionally distributed between the series coupling transformer and the impedance of the supply system. Since the supply system impedance is much smaller than the impedance introduced by the series compensator (transformer impedance plus reflected impedance of the series low-pass filter), a considerably bigger portion of the supply voltage drops across the primary of the transformer. In the case of a stiff supply, it can be considered that all the supply voltage is applied across the primary of the series coupling transformer. However, usually the rated voltage of the transformer primary winding may not be higher than 50% of the supply nominal voltage (bigger ratings may not be practical [3, p. 350]). Thus, during the load side short circuit, the primary of the series coupling transformer experiences full referred phase voltage, which is reflected in the secondary side of the transformer and series VSI. In such circumstances, even if the series VSI is disabled, it acts as a diode rectifier, and the DC capacitor will rapidly charge beyond the voltage ratings of the DC capacitor and the series VSI switches. Thus, the protection circuit should be able to clamp the voltage across the secondary of the series coupling transformer.

series compensator reverses its injected voltage polarity so as to minimise the current flow. This control strategy is schematically presented in Fig.4.2.

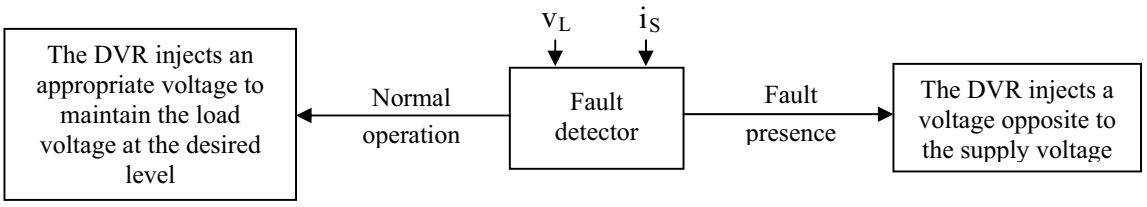


Fig.4.2. Control strategy for protection based on additional control function

The protection schemes proposed in [54, 72] ensures that the VSI switching devices are protected from excessive high current without additional circuit complexity. However, this protection approach can only be applied when the nominal voltage of the primary winding (connected to the grid) of the series coupling transformer is very close to the nominal voltage at the point of common coupling of the UPQC. In other words, this means that the series coupling transformer will have an increased rating that can appear to be uneconomical [3].

In this chapter a protection scheme based on a pair of antiparallel connected thyristors is proposed. Since the proposed scheme does not use varistors for clamping the secondary voltage of the series coupling transformer, this solution does not suffer from the drawbacks mentioned above for the solutions proposed in [55-56]. The thyristors are governed by a very simple Zener diode based control circuit, which does not require separate power source. The overvoltage across the secondary of the series coupling transformer is detected by this control circuit and clamped by a couple of antiparallel thyristors. The protection

Although the protection schemes proposed in [55-56] are simple and easy to implement, and have no interference with the power distribution system protection, the use of varistors causes some disadvantages. As mentioned in [55], varistors can initially fail in a short circuit mode when subjected to surges beyond their peak current/energy ratings. Also, they may fail in a short circuit when operated at steady-state voltages well beyond their ratings values. This mode of stress may result in an eventual open circuit of the device due to the melting of the lead solder joint. When the varistor is in open circuit, the current flowing through it is zero, and the control circuit that generates the gating signals for the thyristors (proposed in [55]) will not generate any signal. If the varistor circuit is open and the thyristor couple is in the off state, large overvoltage will appear across the secondary of the coupling transformer, which will be applied to the series VSI. Another drawback of this protection scheme is failure to protect the series VSI from overcurrent in the situation where the short circuit on load side occurs when the supply system is simultaneously undergoing a deep voltage sag. In this case, the supply voltage may appear to be lower than the reference voltage at which the varistor clamps. Since the varistor does not clamp, the gate signals for thyristors are not generated, and the protection does not divert the short circuit current from the series VSI, which is not disabled. Although in this case, due to utility voltage sag, the short circuit current is reduced it is still much higher than the series VSI ratings.

A different protection approach is proposed in [54, 72], which involves an additional control function combined with the normal operating scheme of the series compensator. The basis of the scheme is that when an overcurrent occurs in the distribution system, the

taken in a reasonably short time interval. Thus, the VSI switches are the most vulnerable to short circuits on the load side of the UPQC, and a special protection has to be designed to protect them from this kind of fault and improve the overall reliability.

The series VSI switches can not be protected from the short circuit current by simply disabling the VSI gate signals or using circuit breakers or fuses. Opening the secondary of the series coupling transformer will result in failure to balance the mmf from the primary winding, which in turn will cause the transformer to be driven into magnetic saturation, and the full referred phase voltage will therefore appear across the secondary winding. Instead, during a short circuit on the load side, a special path must be provided for the flow of the secondary current, which will divert the excessive current from the series VSI switches.

As a path for the secondary current must be provided, the performance of varistors and a pair of thyristors in parallel with the secondary of the series coupling transformer have been investigated in [55-56]. The protection scheme proposed in [55-56] is shown in Fig.4.1

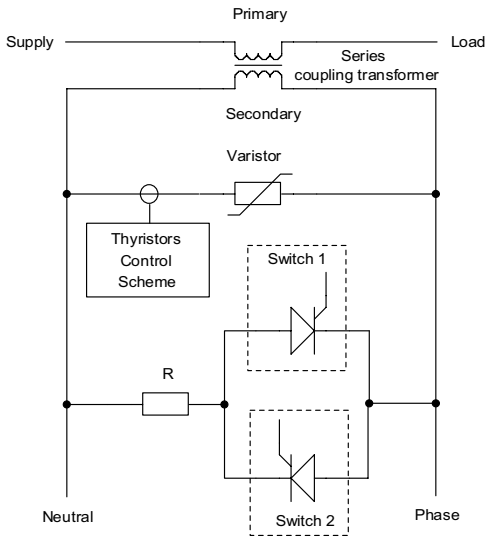


Fig.4.1 Varistor-based protection scheme

Chapter 4

PROTECTION OF UPQC AGAINST THE LOAD SIDE SHORT CIRCUITS

4.1. Introduction

In the previous chapter it has been mentioned that the series converter of the UPQC is connected in series with the electricity supply to provide voltage support in the event of voltage sag/swell or disturbances from the supply side. This presents an imminent danger to the UPQC series inverter when there is excess current flowing from the supply. Such a situation may arise due to several reasons but primarily as a result of short circuits at the load side.

The series VSI is typically connected to the grid through a low-pass filter and a coupling transformer. The compensating voltage is injected in series with the source by means of the primary of the coupling transformer. Normally, this transformer operates like a current transformer and hence its secondary circuit must always be closed by some means. During normal operation, the path for the flow of the secondary current is provided by closing the series VSI switches. However, during a short circuit on the load side, the current flowing through the secondary of the series coupling transformer and hence through the series VSI switches is well above their ratings. Although the series coupling transformer is designed to withstand the short circuit current until the fault is cleared by the system protection, the series VSI switches can be destroyed if proper protection measures are not

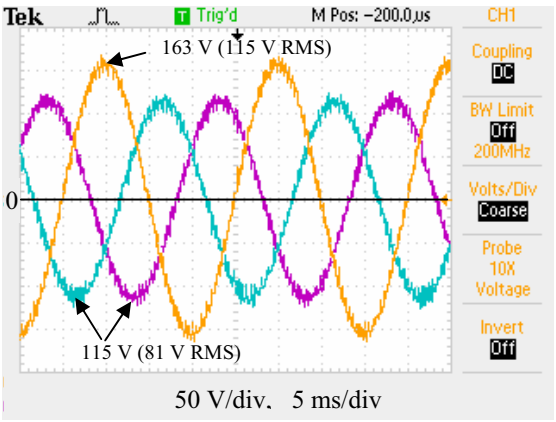
3.7. Summary

This chapter starts with a discussion of the UPQC power circuit structure, principle of operation, design considerations and control strategies. The advantages and disadvantages of different power circuit configurations and control solutions are highlighted. The right-shunt UPQC configuration proved to be superior to the left-shunt UPQC. The *average dc voltage regulation* method, described in sub-section 3.3.1, turned out to be the most attractive control solution, which accomplishes two tasks simultaneously: controls the voltage across the dc link capacitor and determines the amplitude of the supply current. Thus, using this control method the control circuit can by simplified and the number of current sensors reduced. Among different modulation techniques the *hysteresis current control* appears to be the most preferable for the shunt compensator. The hysteresis control method has simpler implementation, enhanced system stability, increased reliability and response speed.

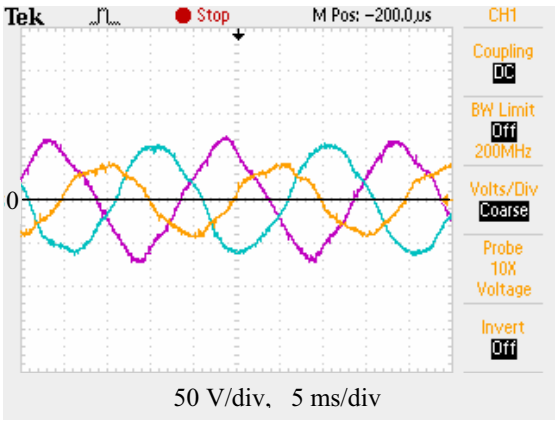
Then, the UPQC simulation study is presented. The simulation model was created in Simulink and greatly assisted in designing the prototype UPQC and developing new control solutions. Using this model, three typical case studies have been simulated, revealing the UPQC steady state and dynamic performance, and its effectiveness in power conditioning.

Finally, the experimental setup and results are presented. As part of the research project a 12 kVA UPQC laboratory prototype has been constructed and tested. The effectiveness of the UPQC has been proved through numerous experimental results obtained with this setup.

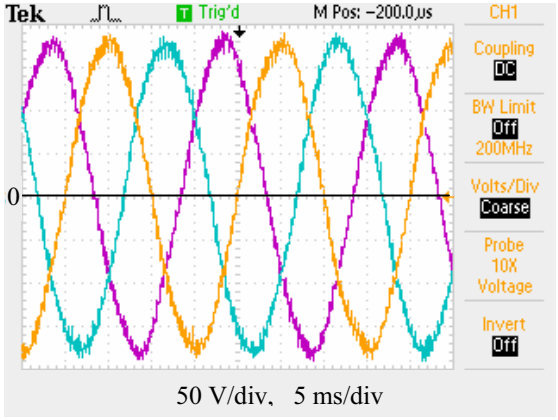
Also, an unbalanced supply voltage sag was created. As we can see from Fig.3.23.a), the supply voltages are unbalanced sinusoids with the magnitudes below the nominal level. Due to proper series injection (see Fig.3.23.b)), the load voltages (see Fig.3.23.c)) are balanced sinusoids (THD=1.7%) with magnitudes equal to 188 V peak, line-to-neutral (corresponding to 230 V rms, line-to-line).



a) supply voltages

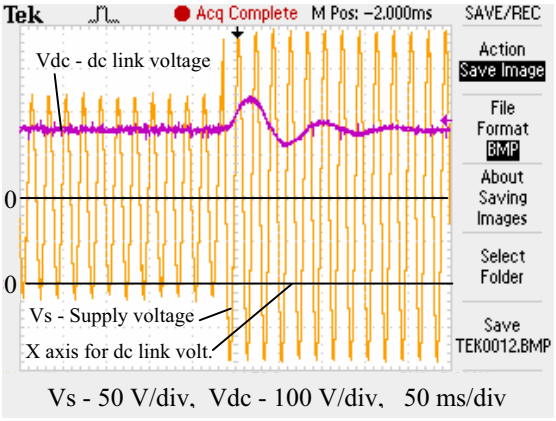


b) injected voltages



c) load voltages (THD=1.7%)

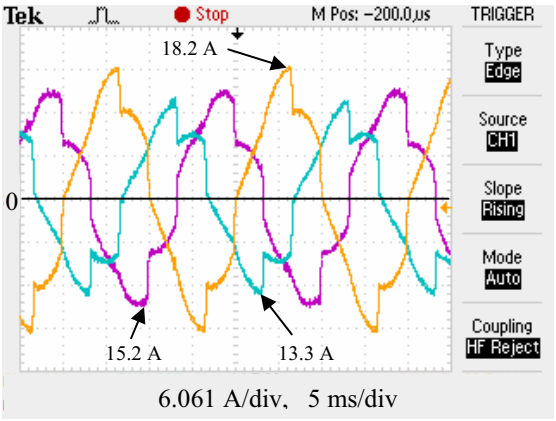
Fig.3.23. Supply unbalance



a) dc link and supply voltages b) dc link voltage and supply current

Fig.3.21. Dynamic performance at supply voltage sag clearance

A load unbalance was created while having normal supply voltages. As we can see from Fig.3.22.a), the load currents are both distorted and unbalanced. However, due to the action of the shunt compensator, the source currents (see Fig.3.22.b)) are balanced sinusoids (containing some acceptable ripple, THD=4.5%).



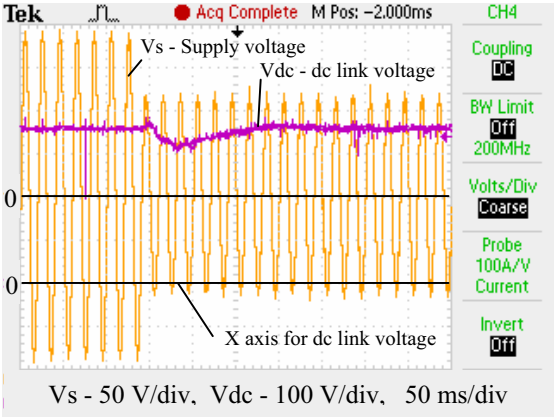
a) load currents b) supply currents (THD=4.5%)

Fig.3.22. Load unbalance

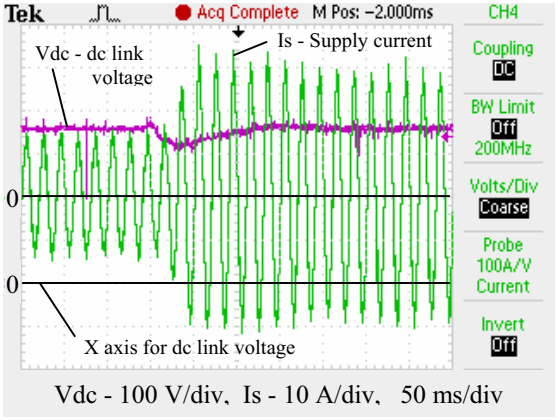
Similarly, the dc link voltage drops down by about 50 V when the nonlinear load is switched on, Fig.3.19.b). In this case, the dc link capacitor is supplying real power to the load until a new supply current reference suitable for new load condition is calculated. In both cases it takes around 14 power cycles for stabilising the dc link voltage.

Fig.3.20 shows the dc link voltage dynamics at supply voltage sag occurrence (a 40% sag has been created). From Fig.3.20.b) we can see that the sag occurrence results in a sudden increase of the supply current. Before a new supply current reference is determined the dc link capacitor is supplying real power to the load causing the dc link voltage drop (about 50 V). After about 6 power cycles the dc link voltage is stabilised.

Fig.3.21 shows the dc link voltage dynamics for clearance of the supply voltage sag created previously. This time, since the supply current decreases, the dc link voltage increases by about 90 V. After about 12 power cycles the dc link voltage is stabilised.



a) dc link and supply voltages

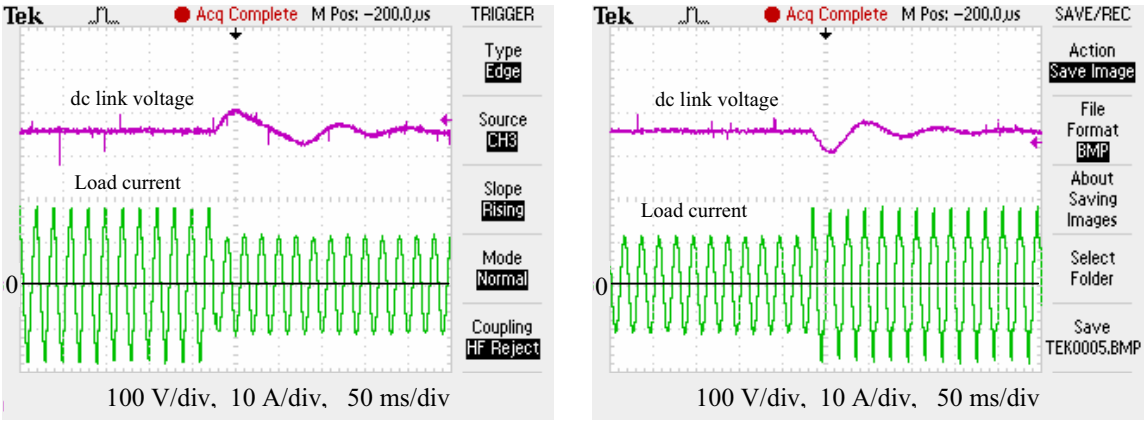


b) dc link voltage and supply current

Fig.3.20. Dynamic performance at supply voltage sag occurrence

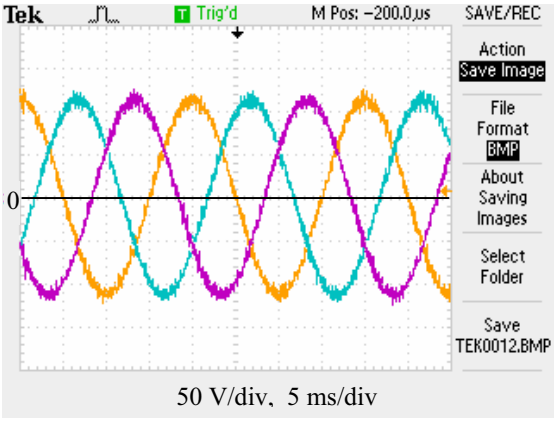
The series compensator is injecting voltages shown in Fig.3.18.b). Due to this series injection the load sees the voltages presented in Fig.3.18.c), which are balanced sinusoids with the magnitude equal to 188 V peak, line-to-neutral (corresponds to 230 V rms line-to-line). The THDs of both the supply (2.3%) and the load (1.5%) voltages are below the 5% limit recommended by IEEE Standard 519-1992. From Fig.3.18.d) we can see that the supply, injected and load voltages are all in phase. Also, from Fig.3.18.e) we can see that the supply voltage and current are in phase which means that no reactive power is drawn from the supply.

In the steady state, by action of a PI controller, the shunt compensator maintains the dc link voltage constant at 350 V (see Fig.3.18.d)). The dc link voltage dynamics after connection/disconnection of the nonlinear load is shown in Fig.3.19. When the nonlinear load is switched off, the real power supplied to it previously is transferred to the dc link capacitor until a new supply current reference suitable for new load condition is calculated. Therefore the dc link voltage rises above the reference value (up to 400 V), Fig.3.19.a).

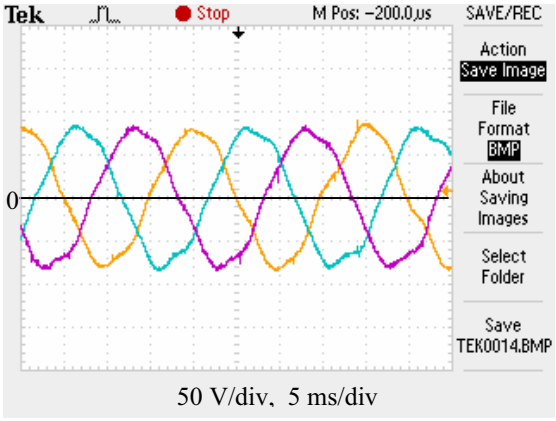


a) disconnection of nonlinear load b) connection of nonlinear load

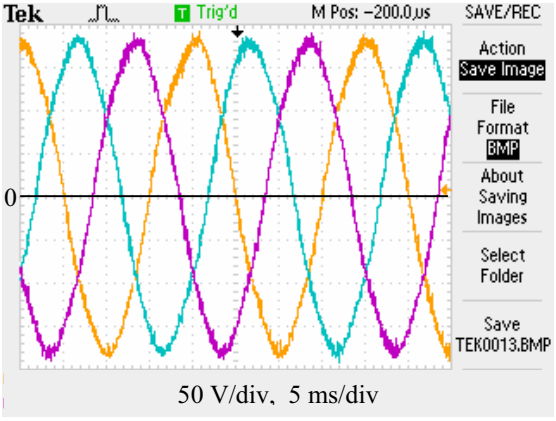
Fig.3.19. Dynamic performance at load change



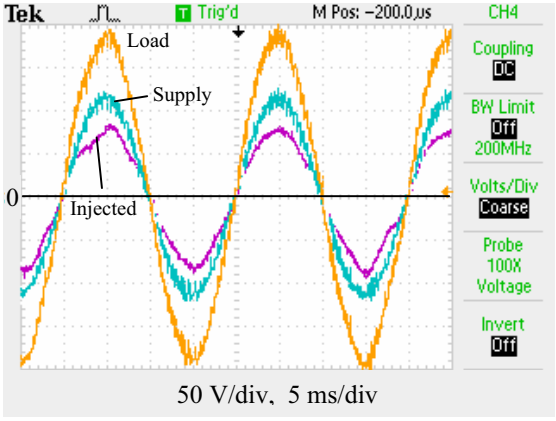
a) supply (THD=2.3%)



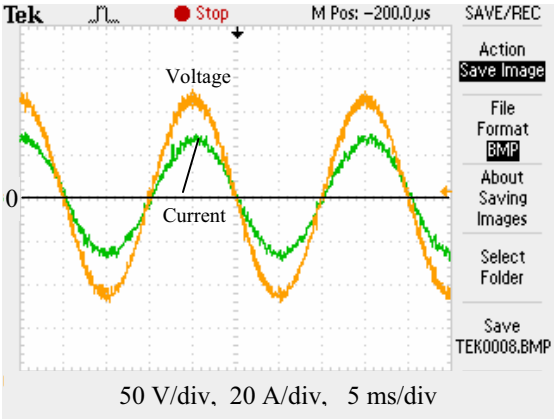
b) injected



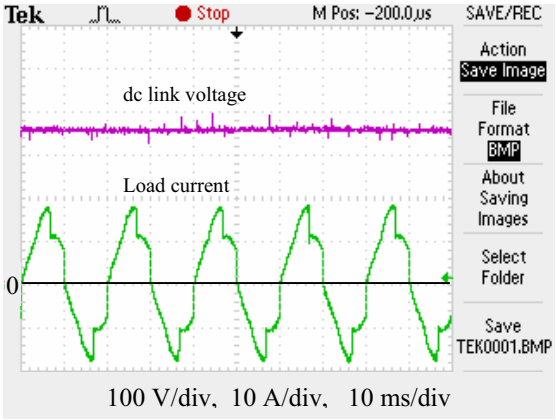
c) load (THD=1.5%)



d) supply, injected and load, phase a



e) supply voltage and current, phase a



f) dc link voltage and load current phase a

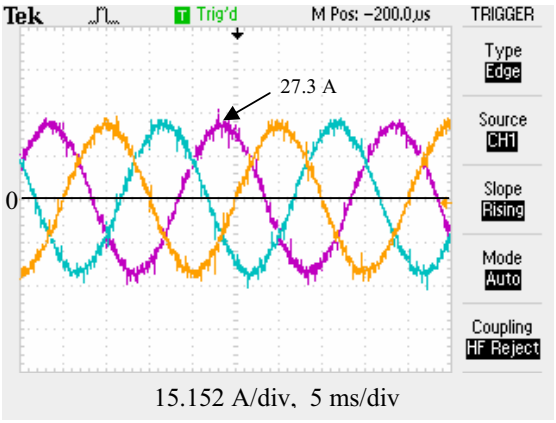
Fig.3.18. Voltages

The measurements have been performed using a Tektronix oscilloscope, type TPS 2024. The results presented in Fig.3.16, Fig.3.17 and Fig.3.22 have been obtained using LA205-S current transducers produced by LEM (see www.lem.com). In Fig.3.16, 1 A corresponds to 66 mV. In Fig.3.17 and Fig.3.22, 1 A corresponds to 33mV. The number of A/division, V/div and time/div are specified at the bottom of each photograph taken of the oscilloscope display.

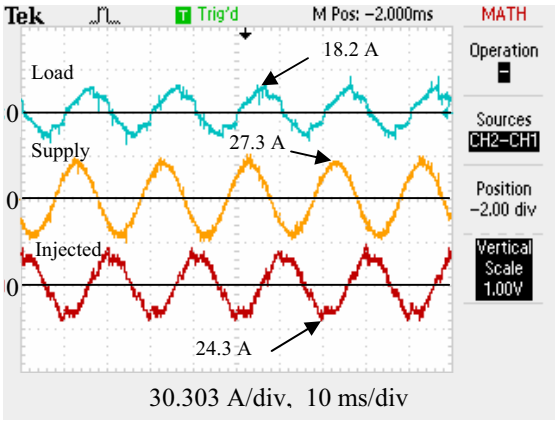
Three loads are connected to the UPQC: resistive (Fig.3.16.a)), inductive (Fig.3.16.b)) and nonlinear (resistor connected to three phase diode bridge rectifier, Fig.3.16.c)). The total load currents are shown in (Fig.3.16.d)).

A 40% supply voltage sag has been created. The supply voltages are shown in Fig.3.18.a).

In Fig.3.17.a) the supply currents are shown. As we can see, these are balanced sinusoids containing some insignificant ripple (THD=4.45%, whereas the limit recommended by IEEE Standard 519-1992 is 8%). In Fig.3.17.b) the supply, load and injected currents of phase a are plotted together.



a) supply (THD=2.8%)

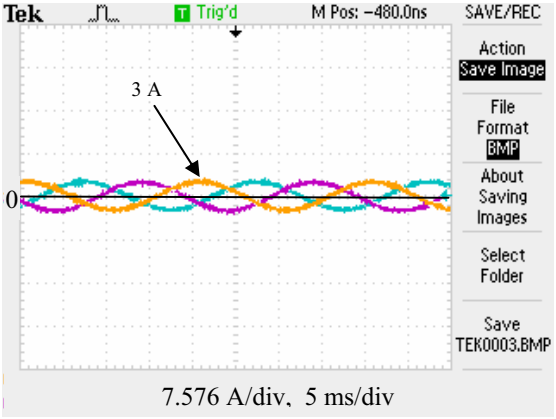


b) supply, injected and load, phase a

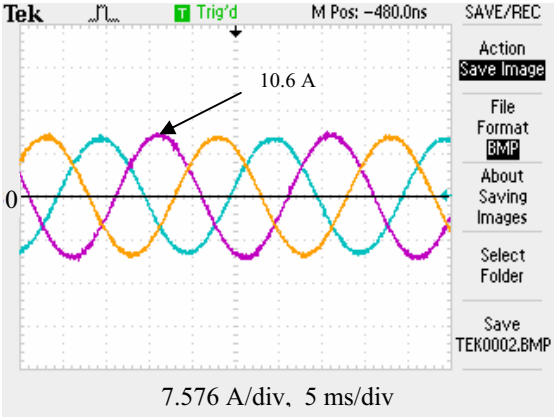
Fig.3.17. Supply, injected and load currents

3.6. Experimental results

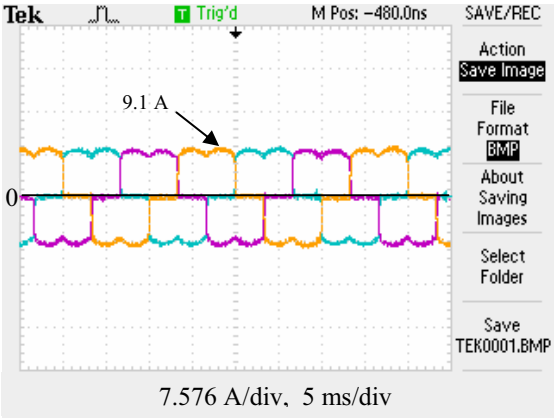
With the prototype UPQC presented in previous section the following experimental results have been obtained. The nominal supply voltage of the experimental setup is 230 V rms line-to-line. An ac power source of type 4500Ls produced by California Instruments has been used throughout the experiment.



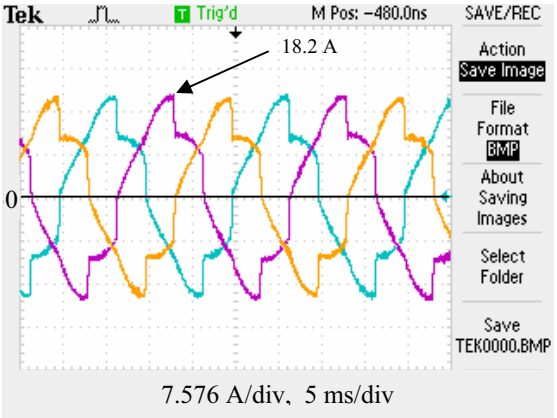
a) resistive load



b) inductive load



c) nonlinear load (THD=21.3%)



d) total load (THD=15.8%))

Fig.3.16. Load currents

3.5.4. Testing

The no-load and short-circuit tests have been carried out for determination of series and shunt coupling transformers parameters, and the results are presented in Appendix C. These tests have shown that both series and shunt transformers have non-linear magnetising characteristics. Some unbalance is observed in transformer parameters. Different phases have slightly different series and parallel impedances and magnetising characteristics.

Also, for a series coupling transformer a special no-load test has been carried out. An increased voltage of up to 180 V has been applied to the winding that is connected to the grid (115 V) and the peak magnetising current has been measured. The results of this test have been used for building up the magnetising characteristic, required by the Simulink non-linear transformer model.

For the purpose of testing the shunt compensator, an analog hysteresis controller has been built. The circuit diagram, printed circuit board (PCB) layout and a photograph of this controller together with the test results are presented in Appendix D. This controller was used in developing and debugging the software for DSP based hysteresis controller.

The series compensator has been tested using a sinusoidal PWM analog controller built by a project colleague.

The UPQC as a whole has been tested using a DSP based controller and the results are presented in the following section.

at the level of 350 V. The *average dc voltage regulation* technique presented in subsection 3.3.1 is applied for dc link voltage regulation and calculation of the supply reference current. The parameters of the PI controller are: $K_P = 0.173\ A/V$, $K_I = 4.82\ A/(V \cdot rad)$. First, these were calculated applying the Ziegler-Nichols tuning rules [22], and then adjusted through experiments. The hysteresis current controller is used for the shunt inverter, which keeps the tracked current within the hysteresis band of ± 0.45A, resulting in an average switching frequency of around 4 kHz.

3.5.3. Construction

The prototype UPQC construction has been performed in the following sequence:

- Procurement of cabinet, components, materials and tools;
- Components testing;
- Components mounting;
- Wiring and marking;
- Insulation testing.

All the above listed tasks have been accomplished by author. Pictures of the prototype UPQC at different assembling stages are presented in Appendix B. This work on the prototype UPQC construction, involved practical experience and required manufacturing skills such as mounting, assembling, wiring and testing.

The measurement interface cards and the card used for interfacing the DSP with the inverters gate drive cards were built by project colleagues.

Circuit breakers and contactors

The UPQC can be disconnected from both the supply side and the load side by operating the dedicated circuit breakers, placed respectively at the input and output of the UPQC. These two circuit breakers also protect the UPQC from internal and load side faults.

One three-phase contactor (Sa_se, Sb_se, Sc_se) is used for bypassing the series active filter, and another contactor (Sa_sh, Sb_sh, Sc_sh) is used for disconnecting the shunt active filter from the grid.

3.5.2. Control scheme

Texas Instrument TMS320F2812 DSP kit performs the coordinated master control and the individual control of the series and shunt compensators. This makes the control circuit flexible. Various control algorithms can be applied without introducing significant changes in the control circuit hardware, if at all. The control technique is changed at the software level. Also, with a DSP, the implementation of advanced control techniques, which involve sophisticated computations, is possible.

The series inverter is controlled to compensate for sags and unbalance in the supply voltage. The fundamental of the injected voltage is in-phase with the supply current. The carrier-based sinusoidal PWM technique is used for the series inverter, and the switching frequency is 18 kHz.

The shunt inverter is controlled to compensate for unbalance, reactive and harmonic components of the load current and to maintain the average voltage across the DC capacitor

shunt filter capacitor. This resistor plus proper choice of shunt inverter switching frequency (hysteresis band) help avoid resonance at switching frequencies.

Measuring devices

Four analogue voltmeters and three analogue ammeters have been mounted on the front panel. One voltmeter indicates the voltage across the dc link capacitor Cdc; the other three (one per phase) measure the voltages injected by the series compensator. The ammeters (one per phase) measure the currents injected by the shunt compensator.

Two three-phase digital multimeters (MULTILED S and MULTILED L) type *M812-LD9* produced by *Multitek Ltd* (see [83]) have been mounted on the front panel: one for supply and another one for load. These two multimeters are used for measuring and displaying the phase and line volts, phase amps, frequency, active, reactive and apparent powers, active and reactive energies, power factor, voltage and current distortions, and other parameters. Current transformers (in each phase) are used for connecting the multimeters. The transformation ratio is 60/5.

LA 205-S transducers produced by LEM (see [84]) are used for measuring the supply and load currents. Transducers output signals used for control purposes are brought into the DSP controller through the current measurement interface card.

The supply, load and dc link voltages are brought into the DSP controller through the voltage measurement interface card.

Filter inductors

The filter inductors of both shunt and series compensators (respectively La_sh, Lb_sh, Lc_sh and La_se, Lb_se, Lc_se) have the following parameters: *L=1.245 mH and R=0.1* Ω.

The inductors have been constructed using iron powder core type E450-33 produced by Micrometals Inc (see [82]). Iron powder is typically used to produce high "Q" inductors and it is a preferred core material due to its stability, high "Q" frequency response, and power handling capabilities.

Filter capacitors

The filter capacitors connected in star on the secondary side of the series transformers (Ca_se_130, Cb_se_130, Cc_se_130) are of 10 μF, and those connected across the primary of the series transformer (Ca_se_115, Cb_se_115, Cc_se_115) are of 300 μF value. This level of capacitance is required across the primary of the series transformer to cancel out the low frequency harmonics, which appear in the injected voltage, mostly due to the blanking time during commutation of the series inverter switches.

The filter capacitors of the shunt compensator (Ca_sh, Cb_sh, Cc_sh) are of 20 μF level and they are connected in delta which triples the capacitance per phase comparative with star connection. Thus, due to the delta connection, the effective capacitance per phase is 60 μF. A 4 Ω damping resistor (Ra_sh, Rb_sh, Rc_sh) is connected in series with each

Table 3.2: Transformers parameters (series / shunt)

Parameters	Series	Shunt
Number of phases	Single-phase	Three-phase
Power, kVA	4	12
Voltages (primary / secondary), V	115 / 130	230 / 130
Core Resistance, Ω	363.7	1547.3
Core inductance, mH	945	10441
Winding resistance, Ω	0.1322	0.1588
Winding leakage inductance, mH	0.42	0.1684

The transformers are connected with their primary windings to the grid. The shunt autotransformer windings are connected in star. The transformer no-load tests have shown that both the shunt and series transformers have non-linear magnetizing characteristics. For the shunt converter this may not be an issue, since the magnetising current (which is nonlinear) is only a small fraction (up to 5%) of the nominal transformer current and it cannot seriously distort the injected current waveform. However, the nonlinearity of the series transformers magnetising characteristics has to be considered. Since the supply current (which passes through the series transformer) is controlled to be sinusoidal, due to nonlinearity of the magnetising characteristics, the voltage injected by the series transformer will contain unwelcome harmonics. Among these, the most significant is the third harmonic. The cores of those three single-phase series transformers do not form a three-phase magnetic system, therefore, their magnetic fluxes are independent from each other and do not sum up to zero, allowing the triplen harmonics to exist. Thus, in order to remove the triplen harmonics, the secondary windings of the series transformers are connected in delta. Also, the delta connection of the inverter side windings maximises the utilisation of the dc link voltage [75].

Inverters

The series and shunt inverters have been bought from *SmartPower ATE Ltd* (see [81]). These are standard 6-switch voltage source inverters based on *TOSHIBA MG150J2YS50* IGBT devices. The series inverter is operated under voltage control mode and the shunt under current control mode. An interface card is used for matching the switching signals generated by DSP with the inverters gate drive cards.

dc link

Across the dc link a 2200 μF, 500 V electrolytic capacitor is connected (Cdc). Two two-pole switches (Sw_dc_se and Sw_dc_sh) are used for connecting/disconnecting the dc link capacitor Cdc to/from the series and shunt inverters respectively.

Coupling transformers

Three identical single phase transformers (Ta_se, Tb_se, Tc_se) are used for interfacing the series inverter with the grid. The shunt inverter is interfaced through a three-phase autotransformer (phases are marked Ta_sh, Tb_sh, Tc_sh). The parameters of the series and shunt coupling transformers are determined through no-load and short-circuit tests and are given in Table 3.2. The resistances and inductances are calculated based on transformer primary winding voltage (115 V for series and 230 V for shunt).

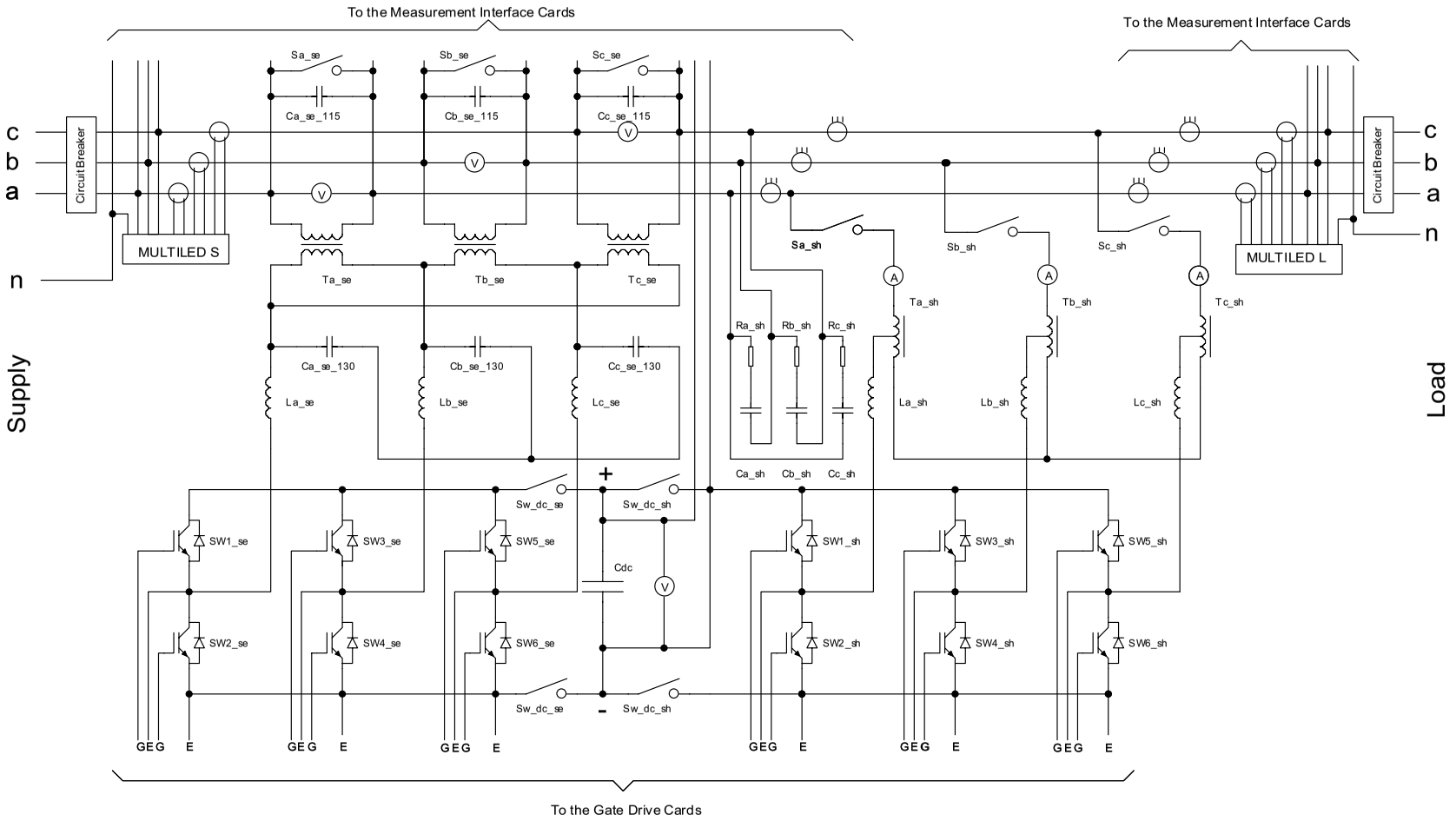


Fig.3.15. Power circuit layout of the prototype UPQC

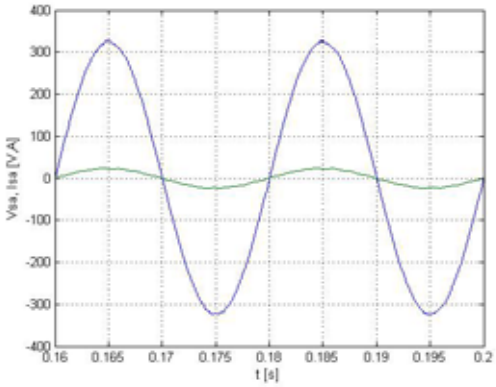
3.5. Prototype UPQC

At the beginning of the previous section the role and importance of computer simulation in the analysis and design of power electronic systems have been mentioned. However, computer simulations should not be looked upon as a substitute for a hardware prototype. It should be mentioned that in power electronics computer simulation and a hardware prototype are complimentary to each other. Thus, it is important to have both the simulation model and hardware prototype. As a part of the Unified Power Quality Conditioner (UPQC) research project, carried out between February 2005 and May 2008 at the School of Electrical Engineering Systems, Dublin Institute of Technology, a 12 kVA UPQC laboratory prototype has been constructed and tested.

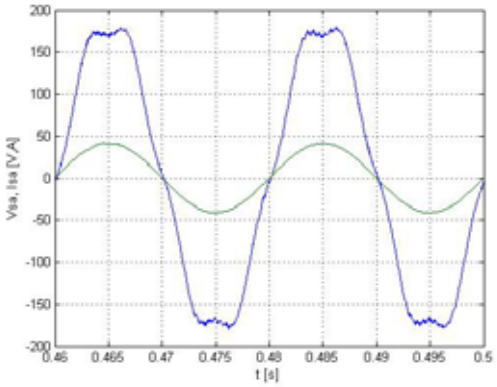
3.5.1. Power circuit configuration and components parameters

The prototype UPQC is intended to be used in three-phase three-wire systems, therefore it cannot provide compensation for zero-sequence components. The right-shunt compensation configuration is used with the prototype UPQC. The ratings of the prototype UPQC are: 230 V (line-to-neutral) and 17.4 A for the shunt compensator, and 115 V and 34.8 A for the series compensator. The power circuit layout of the prototype UPQC is shown in Fig.3.15.

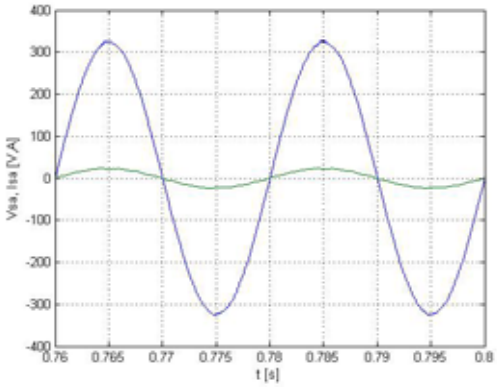
Due to unity power factor compensation, throughout the entire simulated period, the supply current is in-phase with the fundamental of the supply voltage (see Fig.3.14), which means that no reactive power is drawn from the supply.



a) before sag



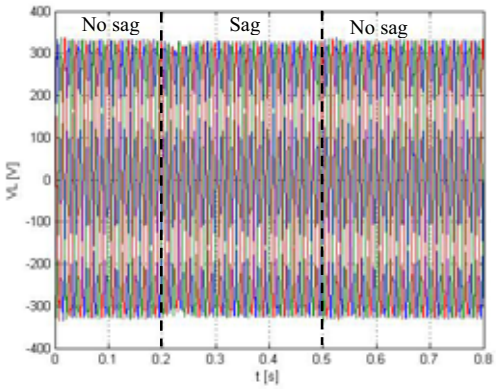
b) during sag



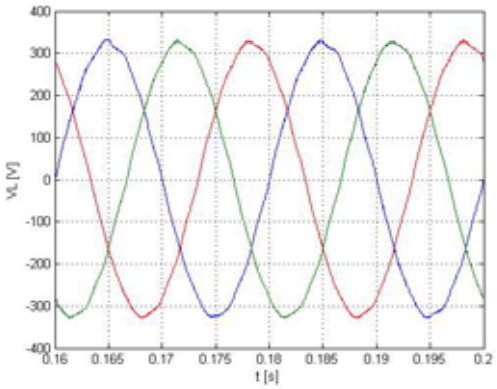
c) after sag clearance

Fig.3.14. Simulation results for case study 3: supply voltage and current, phase a

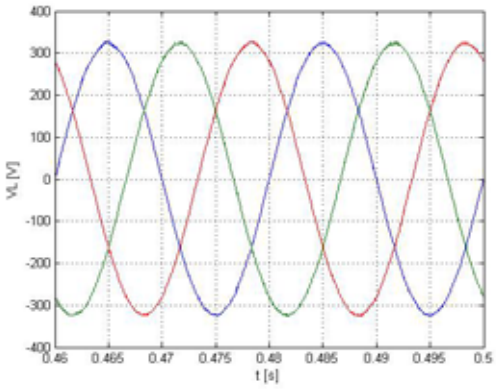
transient periods during which the dc link capacitor is supplying/absorbing active power in order to ensure the power balance. Due to this transient supply/absorption of active power, the dc link voltage is undergoing a sag during the time interval 0.2 s – 0.4 s, and a swell during the interval 0.5 s – 0.7 s. From Fig.3.12.b) we can see that after the transients die out the dc link voltage is restored back to its reference value (400 V).



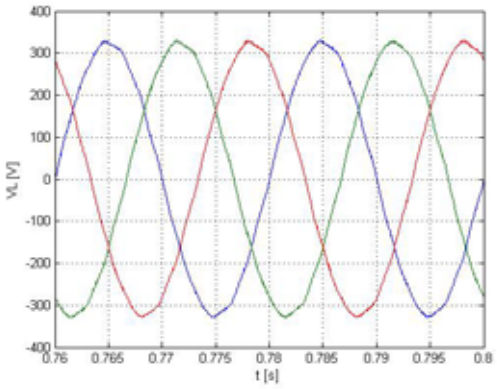
a) load voltage dynamics



b) before sag (THD=1.4%)



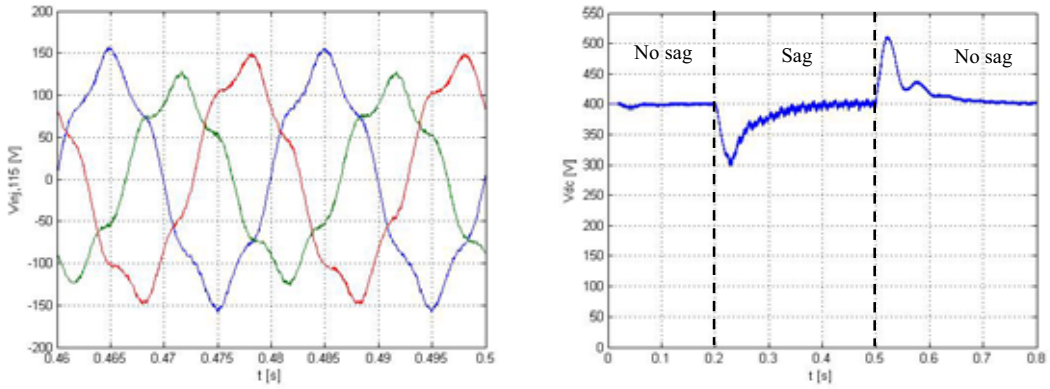
c) during sag (THD=0.75%)



d) after sag clearance (THD=1.4%)

Fig.3.13. Simulation results for Case Study 3: load voltages

During the supply voltage sag, the series compensator is injecting voltages shown in Fig.3.12.a), and due to this series compensation the voltages on the load side are balanced sinusoids (see Fig.3.13.c)), having the THD=0.75%, which is much below the 5% limit recommended by IEEE Standard 519-1992. From Fig.3.13 we can see that throughout the simulation time interval the load voltages are kept at the nominal level, 325 V peak, corresponding to 230 V rms.

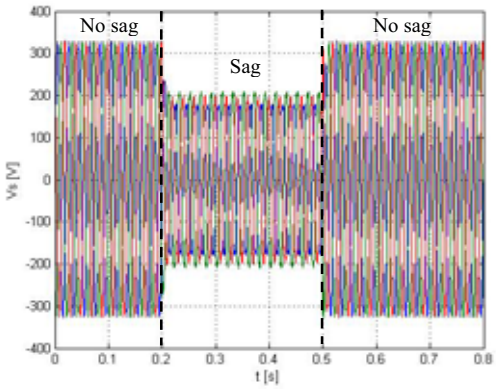


a) voltages injected during sag b) dc link voltage

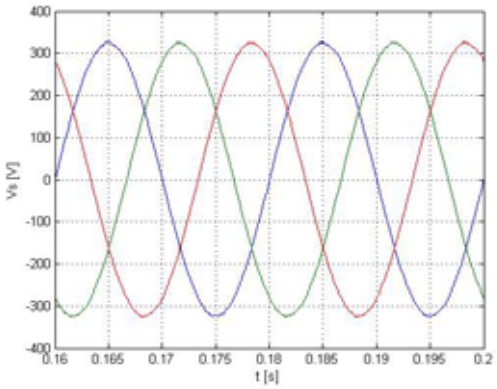
Fig.3.12. Simulation results for case study 3: injected and dc link voltages

The dc link voltage dynamics are shown in Fig.3.12.b). Due to occurrence/clearance of the supply voltage sag, at 0.2 s the supply current is increased and at 0.5 s it is decreased. Since it takes a finite time interval to calculate the new reference current, the shunt compensator cannot immediately response to this supply current change. Also, some settling time is required to stabilise the controlled parameter around its reference. Consequently, after the sag occurrence/clearance instants (0.2 s and 0.5 s) there exist some

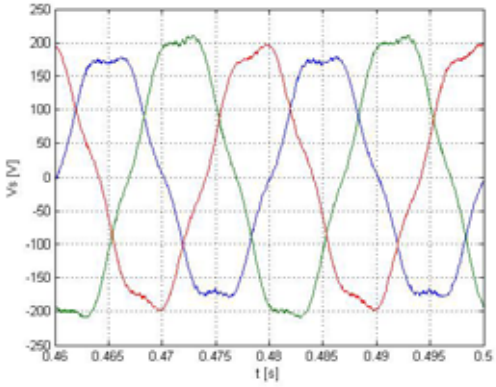
The supply voltage dynamics are shown in Fig.3.11.a). During the sag condition (from 0.2 s to 0.5 s) the supply voltages are undergoing a 30% sag. On top of this, they are unbalanced and distorted (THD=7.7%), Fig.3.11.c). During the other two sub-intervals (from 0 s to 0.2 s and from 0.5 s to 0.8 s) the supply voltages are balanced sinusoids at nominal level (325 V peak, corresponding to 230 V rms), Fig.3.11.b) and Fig.3.11.d).



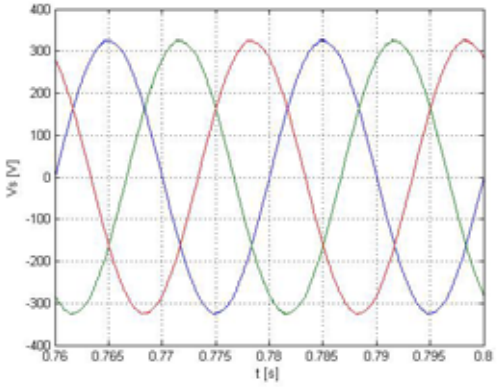
a) supply voltage dynamics



b) before sag (THD=0.55%)



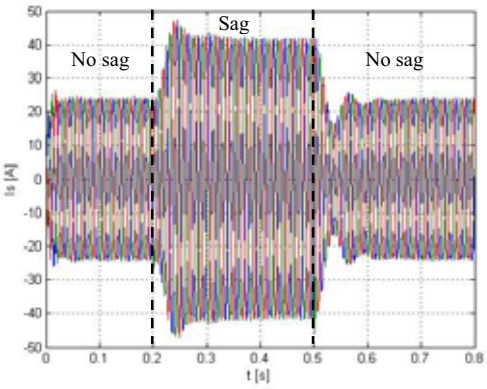
c) during sag (THD=7.7%)



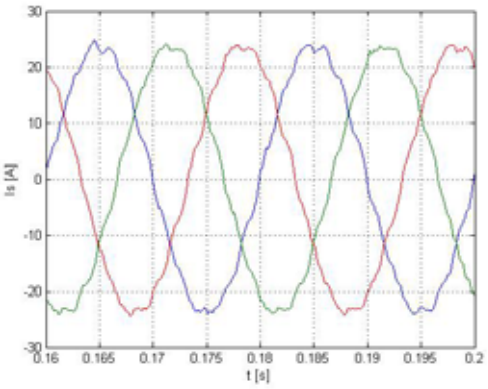
d) after sag clearance (THD=0.55%)

Fig.3.11. Simulation results for Case Study 3: supply voltages

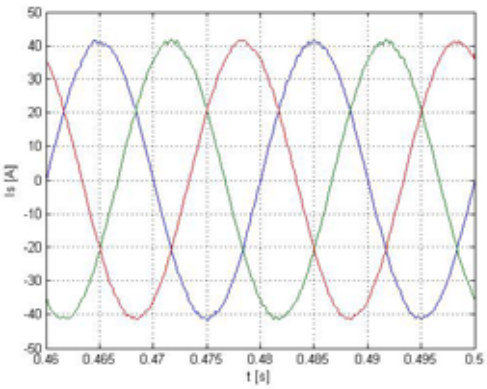
After the supply voltage sag occurrence/clearance the system goes through a transient period after which the supply currents become balanced sinusoids, Fig.3.10.b) – Fig.3.10.d), and in phase with the supply voltage, Fig.3.14. Thus, the UPQC automatically adjusts the injected current in response to supply voltage sag occurrence/clearance, ensuring that in the steady state the supply currents are always balanced sinusoids and no reactive power is drawn from the supply.



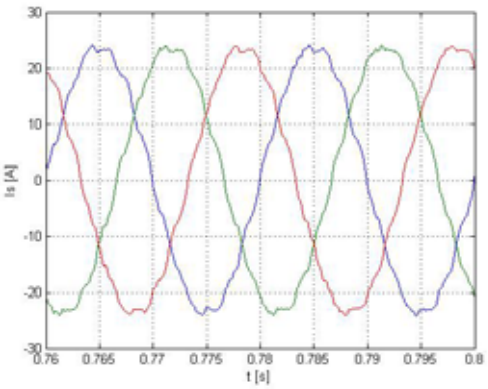
a) supply current dynamics



b) before sag (THD=3.8%)



c) during sag (THD=1.1%)

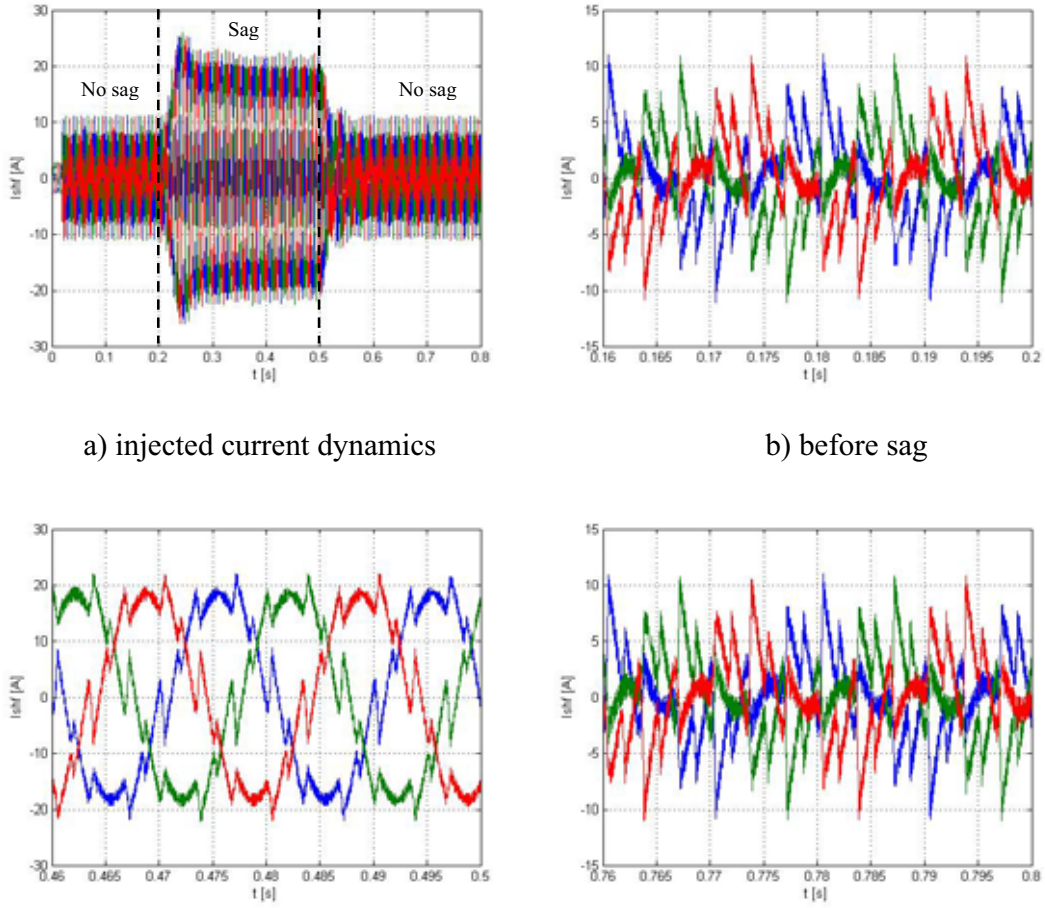


d) after sag clearance (THD=3.8%)

Fig.3.10. Simulation results for Case Study 3: supply currents

current should be accordingly increased in order to provide the same nominal power to the load.

Also, the UPQC is not a lossless device and the power losses associated with it introduce an additional increase in source current.



a) injected current dynamics

b) before sag

c) during sag

d) after sag clearance

Fig.3.9. Simulation results for Case Study 3: injected currents

Case study 3

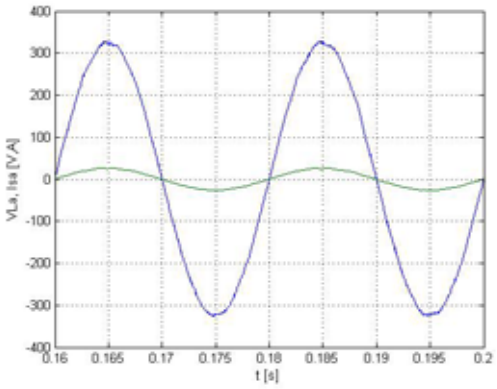
During the entire simulation time interval (from 0s to 0.8 s), only the nonlinear load is connected. The load current profile is the same as shown above in Fig.3.4.b).

A 30% supply voltage sag is created at 0.2 s and cleared at 0.5 s. On top of this, during the same time period, the supply voltages become unbalanced and distorted (the 5th harmonic is present). The supply voltages are presented in Fig.3.11.

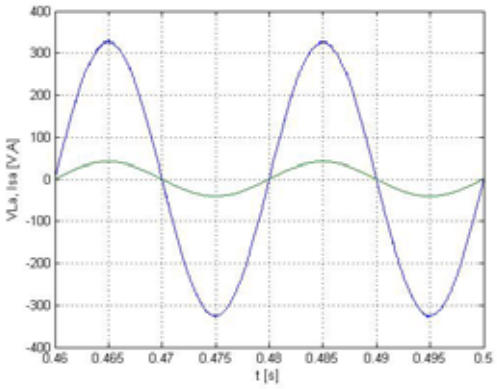
In this case study the UPQC dynamic performance at supply voltage sag occurrence/clearance is investigated and the simulation results are presented in Fig.3.9 through Fig.3.14.

In Fig.3.9 the currents injected by the shunt compensator are shown. Although the load is not changed throughout the simulated time interval, the injected current is considerably increased during the sag condition (from 0.2 s to 0.5s), and this increase is determined by the supply voltage decrease. Since the voltage injected by the series compensator during the sag is in phase with the supply current, in order to make this series compensation possible, the appropriate level of real power has to be transferred from the supply through the shunt converter and dc the link to the series compensator. Due to this real power transfer loop the shunt compensator current increases. For the same reason the supply current is also increased considerably during the sag, Fig.3.10.

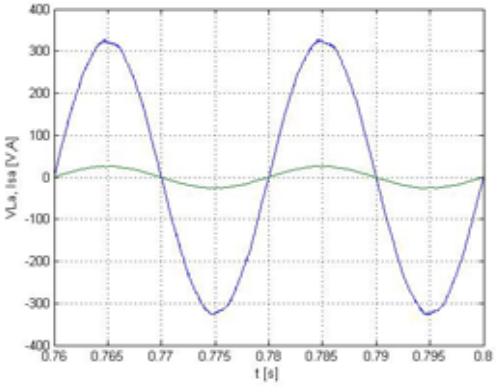
There is also another explanation for this supply current increase. During the sag, the load should draw from the supply the same amount of power as it does in the normal condition (nominal power). Since during the sag the supply voltage is decreased, the supply



a) nonlinear load



b) nonlinear and linear loads



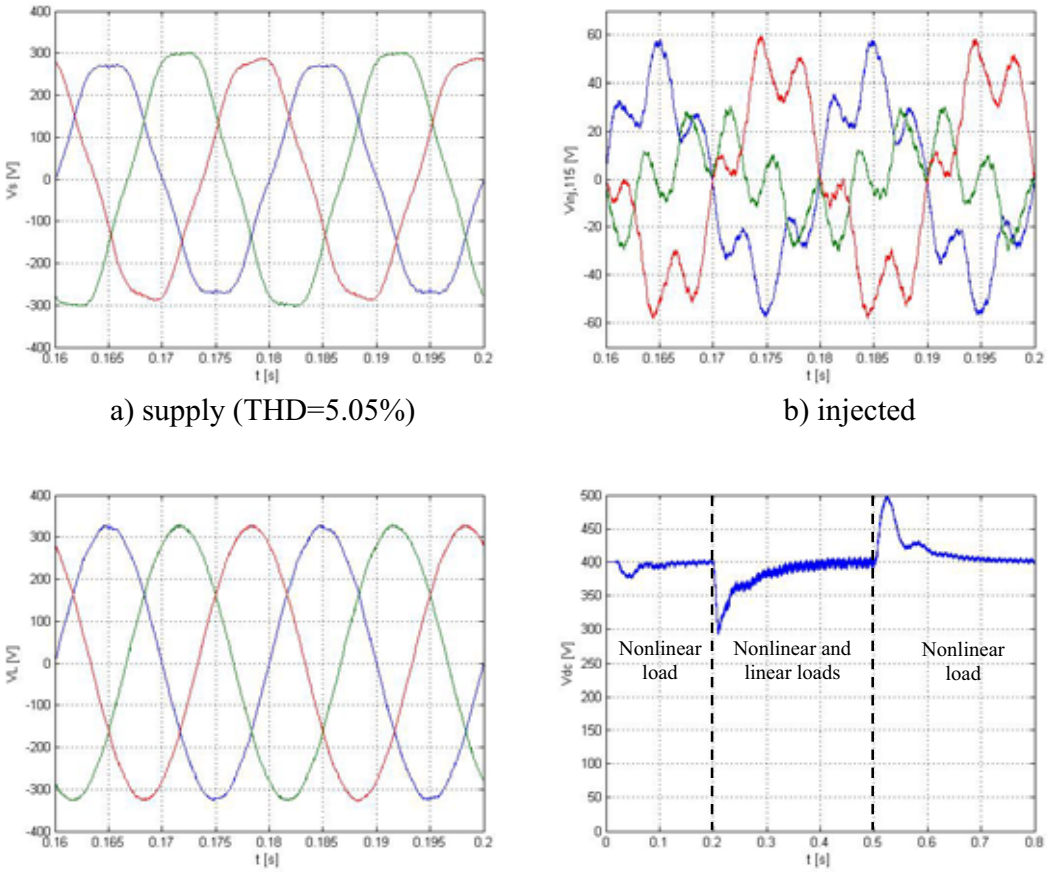
c) nonlinear load

Fig.3.8. Simulation results for Case Study 2: load voltage and supply current, phase a

The dc link voltage dynamics is shown in Fig.3.7.d). At 0.2 s the load current is increased and at 0.5 s it is decreased, due to connection/disconnection of the linear load. Since it takes a finite time interval to calculate the new reference current, the shunt compensator cannot immediately response to the load change. Also, some settling time is required to stabilise the controlled parameter around its reference. Consequently, after the load change instants (0.2 s and 0.5 s) there exist some transient periods during which the dc link capacitor is supplying/absorbing active power in order to ensure the power balance. Due to this transient supply/absorption of active power, the dc link voltage is undergoing a sag during the time interval 0.2 s – 0.4 s, and a swell during the interval 0.5 s – 0.7 s. From Fig.3.7.d) we can see that after the transients die away the dc link voltage is restored back to its reference value (400 V). The issues related to the dc link voltage transients are treated separately in Chapter 6.

The shunt compensator is controlled in such a way that the supply current is in-phase with the fundamental of the supply voltage, which means that no reactive power is drawn from the supply. Also, the fundamental of the series injected voltage is in-phase with the supply current. Thus, the supply current should be in-phase with the load voltage, and this is the case in Fig.3.8.

During the entire simulation period (from 0s to 0.8 s), the supply voltages are unbalanced and distorted (THD=5.05%), and are as shown in Fig.3.7.a). The series compensator is injecting voltages shown in Fig.3.7.b), and due to this series compensation the voltages on the load side are balanced sinusoids (see Fig.3.7.c)), having the THD=1%, which is much below the 5% limit recommended by IEEE Standard 519-1992. From Fig.3.7.c) we can see that the load voltages are kept at the nominal level, 325 V peak, corresponding to 230 V rms.



a) supply (THD=5.05%)

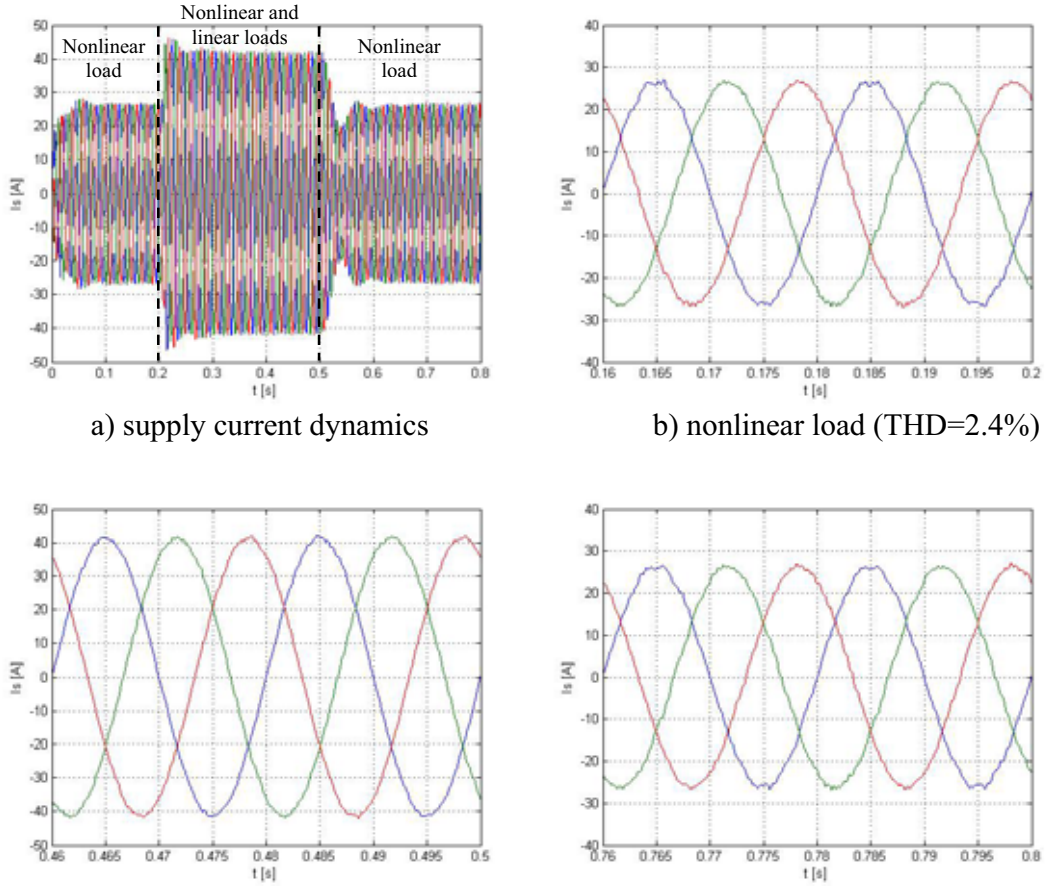
b) injected

c) load (THD=1%)

d) dc link

Fig.3.7. Simulation results for Case Study 2: voltages

From Fig.3.5 and Fig.3.6 we can see that the load current changes are reflected in both injected and supply currents. Following the load change, the system goes through a transient period after which the supply currents become balanced sinusoids, Fig.3.6.b) – Fig.3.6.d), and in phase with the load voltage, Fig.3.8. Thus, the UPQC automatically adjusts the injected current according to the load condition, ensuring that in steady state the supply currents are always balanced sinusoids and no reactive power is drawn from the supply.



a) supply current dynamics

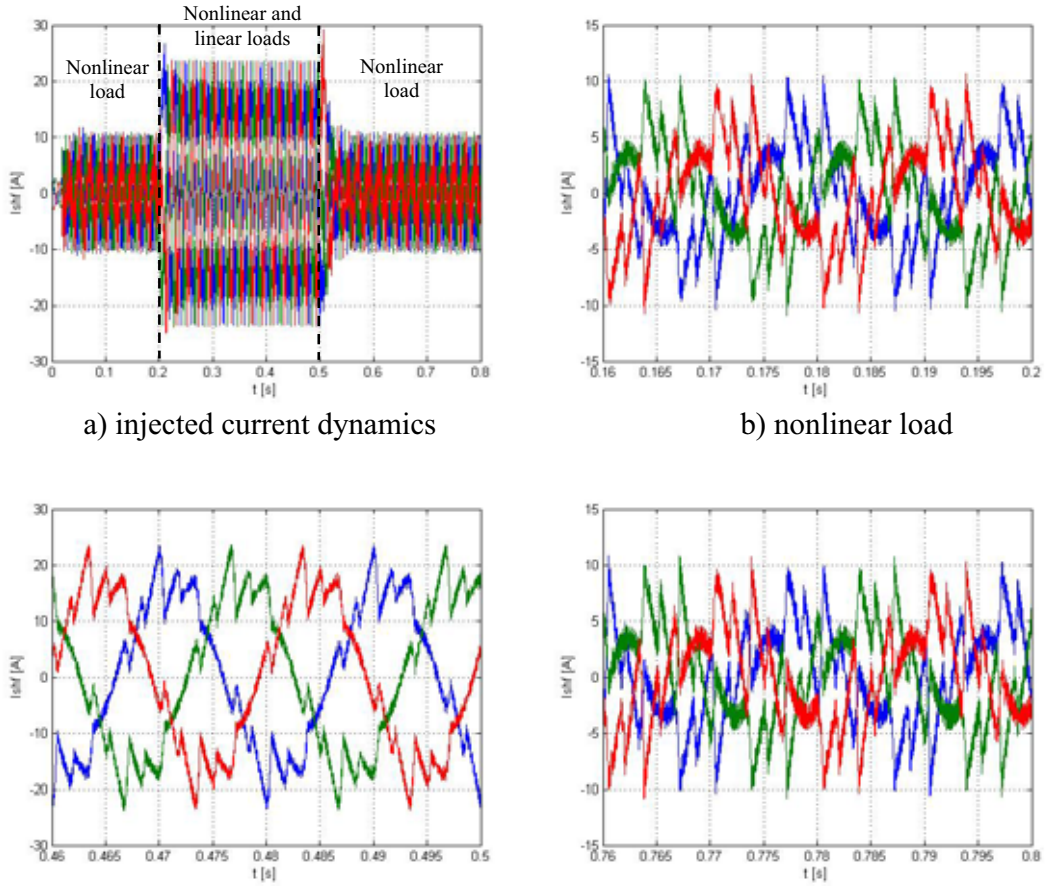
b) nonlinear load (THD=2.4%)

c) nonlinear and linear loads (THD=1.3%)

d) nonlinear load (THD=2.4%)

Fig.3.6. Simulation results for Case Study 2: source currents

Fig.3.4.a) shows how the load current changes during the simulated interval (from 0 s to 0.8 s). As we can see, the simulated interval is composed of three sub-intervals: 1) from 0 s to 0.2 s, when only the nonlinear load is connected; 2) from 0.2 s to 0.5 s, when both the nonlinear and linear loads are connected, and; 3) from 0.5 s to 0.8 s, when again only the nonlinear load is connected. For better viewing, the load current from each of these three subintervals is zoomed in and shown in Fig.3.4.b) through Fig.3.4.d). In the same way, the injected and supply currents are presented in Fig.3.5 and Fig.3.6.



a) injected current dynamics

b) nonlinear load

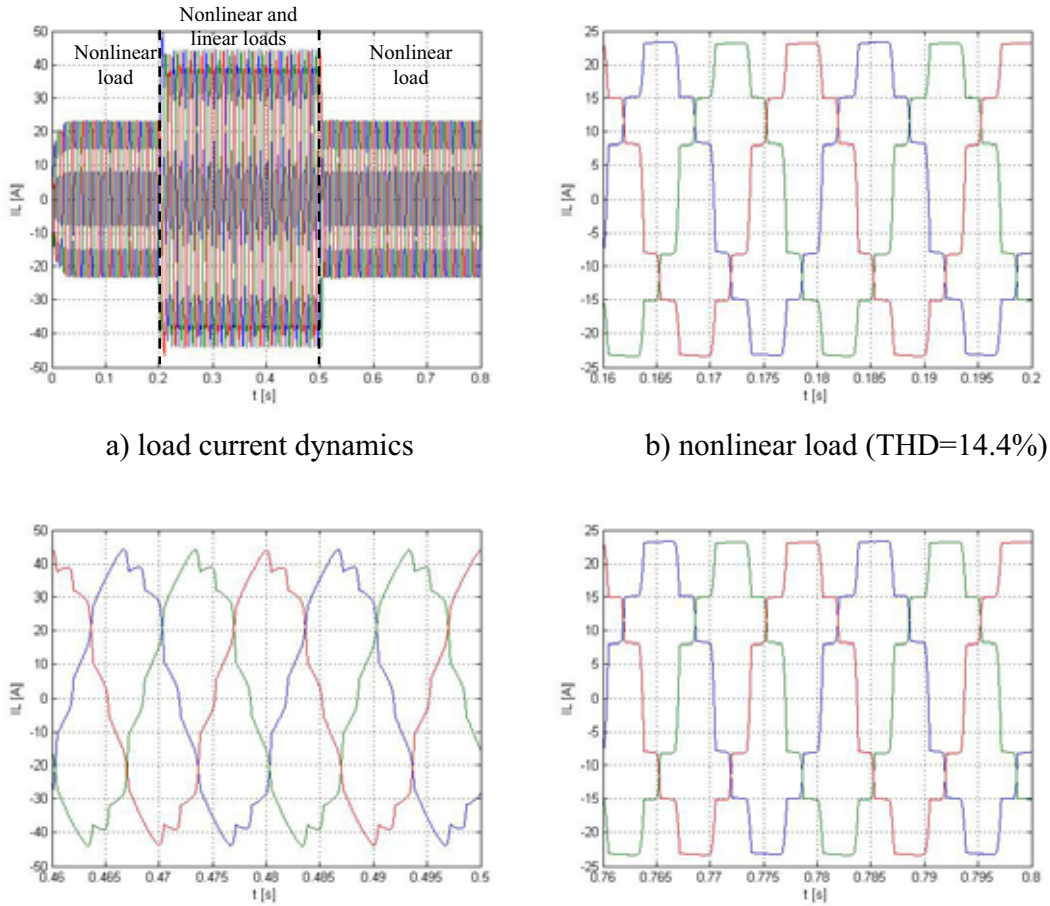
c) nonlinear and linear loads

d) nonlinear load

Fig.3.5. Simulation results for Case Study 2: injected currents

Case Study 2

The supply voltages (see Fig.3.7.a)) are unbalanced and distorted (the 5th harmonic is present), but there is no sag this time. The nonlinear load is permanently connected and the linear load is connected at 0.2 s and disconnected at 0.5 s. In this case study the UPQC dynamic performance at load change is investigated and the simulation results are shown in Fig.3.4 through Fig.3.8.



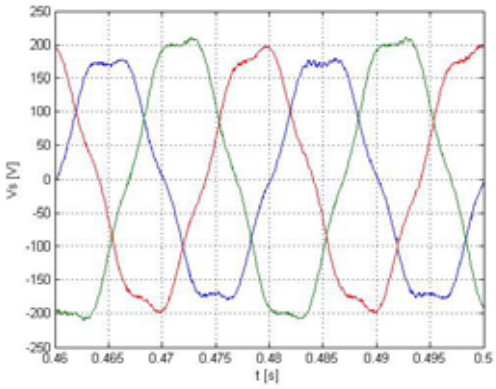
a) load current dynamics

b) nonlinear load (THD=14.4%)

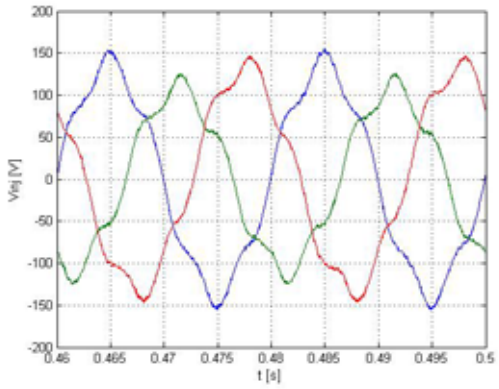
c) nonlinear and linear loads (THD=7.9%)

d) nonlinear load (THD=14.4%)

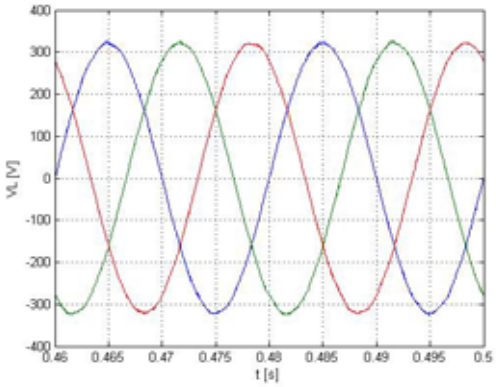
Fig.3.4. Simulation results for Case Study 2: load currents



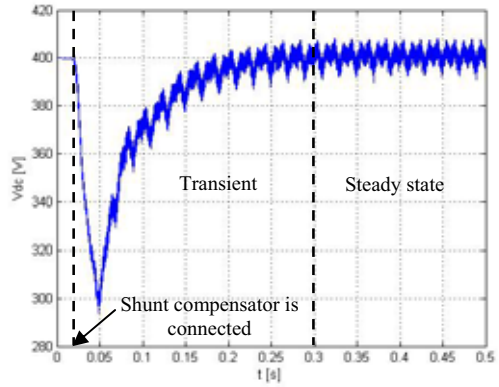
a) supply voltages (THD=7.7%)



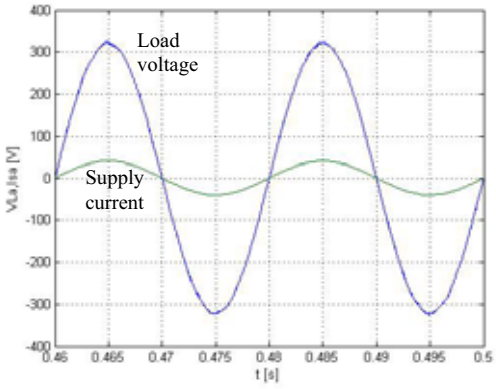
b) voltages injected by series active filter



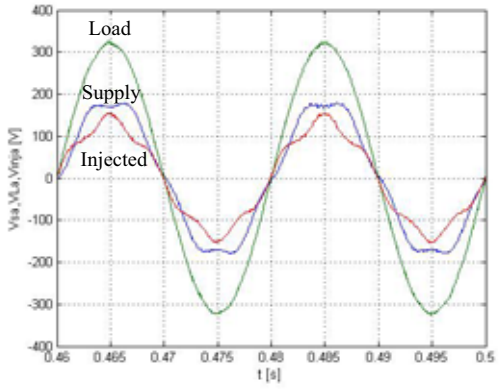
c) load voltages (THD=0.7%)



d) dc link voltage



e) load voltage and supply current, phase a



f) supply, injected and load voltages, phase a

Fig.3.3. Simulation results for Case Study 1: voltages

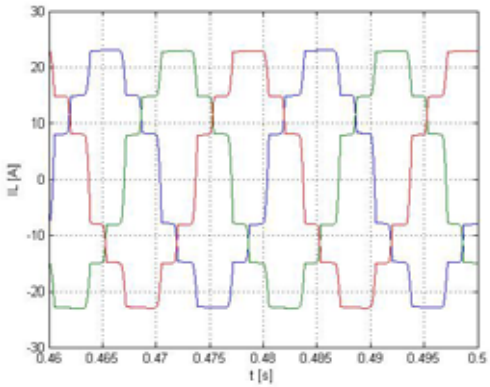
From Fig.3.2.a) we can see that the load currents are highly distorted (the total harmonic distortion (THD) is 14.3%), whereas according to IEEE Standard 519-1992 they should not exceed 8% in our case. Due to the injection of compensating currents (see Fig.3.2.b)), the supply currents (see Fig.3.2.c)) are balanced sinusoids (THD=1.15%), which fulfill the 8% restriction mentioned above. Also, from Fig.3.3.e), it can be seen that the supply current is in-phase with the load voltage, which (due to the in-phase series voltage injection) is in-phase with the fundamental of the supply voltage. Thus, no reactive power is drawn from the supply. In Fig.3.2.d) the supply, load and injected currents of phase *a* are plotted together. On this graph, if the injected current wave is subtracted from the load current wave the result will be the supply current wave.

From Fig.3.3.a) we can see that the supply voltages are unbalanced, distorted (THD=7.7%) and undergoing a sag. The series compensator is injecting voltages shown in Fig.3.3.b). Due to this series compensation the voltages on the load side are balanced sinusoids (see Fig.3.3.c)), having THD=0.7%, which is much below the 5% limit recommended by IEEE Standard 519-1992. From Fig.3.3.c) we can see that the load voltages are kept at the nominal level, 325 V peak, corresponding to 230 V rms. In Fig.3.3.f) the supply, load and injected voltages of phase *a* are plotted together. On this picture, if the injected voltage wave is added to the supply voltage wave the result will be the load voltage wave.

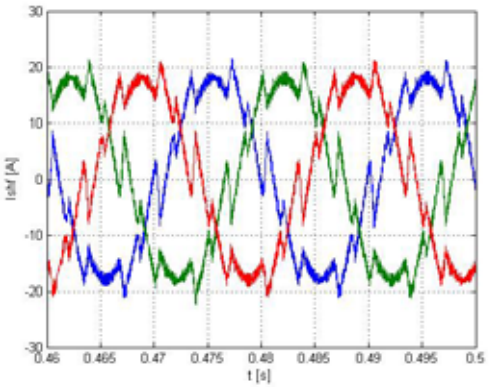
In Fig.3.3.d) the dc link voltage is presented. The shunt compensator is connected at 0.02 s which causes a drop in dc link voltage. After a transient, which lasts from 0.02 s to about 0.3 s, the dc link voltage is restored. As we can see from Fig.3.3.d), in steady state the average dc link voltage is kept at 400 V.

Case Study 1

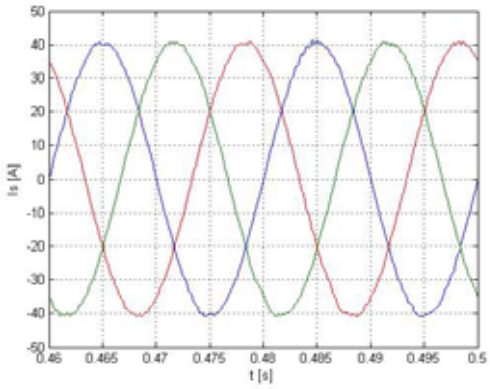
The supply voltages are unbalanced, distorted (the 5th harmonic is present) and undergoing a 30% sag (See Fig.3.3.a)). Of those two loads described above only the nonlinear load is connected in this case study. The UPQC steady state performance is investigated and the simulation results are shown in Fig.3.2 and Fig.3.3.



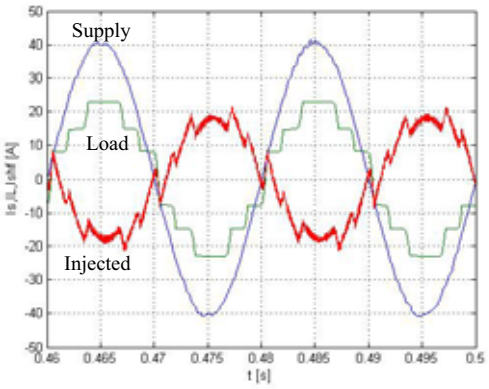
a) load currents (THD=14.3%)



b) currents injected by shunt active filter



c) supply currents (THD=1.15%)



d) supply, load and injected currents, phase a

Fig.3.2. Simulation results for Case Study 1: currents

pu parameters are calculated as required in Simulink, based on transformer power and voltage ratings.

Table 3.1: Transformers parameters (series / shunt)

Rating, kVA	4 (per phase) / 12	
Core Resistance, pu	110 / 117	
Core inductance, pu	90 / 248	
	Primary	Secondary
Voltage, V	115 / 230	130 / 130
Winding resistance, pu	0.02 / 0.006	0.02 / 0.006
Winding leakage inductance, pu	0.02 / 0.002	0.02 / 0.002

The series inverter is controlled to compensate for sags/swells, unbalance and distortion in the supply voltage. The fundamental of the injected voltage is in-phase with the supply current. The UPQC-P control technique described in subsection 3.3.3 is applied for the series compensator. The shunt inverter is controlled to compensate for unbalance, reactive and harmonic components of the load current and to maintain the average voltage across the DC capacitor at the level of 400 V. The *average dc voltage regulation* technique presented in subsection 3.3.1 is applied for dc link voltage regulation and calculation of the supply reference current. The parameters of the PI controller are: $K_P = 0.2\ A/V$, $K_I = 2.8\ A/(V \cdot rad)$ (see Fig.A27 in Appendix A). First, these were calculated applying the Ziegler-Nichols tuning rules [22], and then adjusted through simulations. The hysteresis current controller is used with the shunt inverter, which keeps the tracked current within the hysteresis band of ± 1A (4.4% of the load fundamental current), resulting in an average switching frequency of 5.8 kHz. The switching frequency of the series inverter is 10 kHz.

3.4. Simulation study

Computer simulation has become an indispensable part of the power electronics design process. UPQC is a complex power electronics device and the analysis of its behaviour, which leads to improved understanding, would be very difficult without computer simulations (if possible at all). The overall design process can be shortened through the use of computer simulations, since it is usually easier to study the influence of a parameter on the system behaviour in simulation, as compared to accomplishing the same in the laboratory on a hardware prototype. A UPQC simulation model (see Appendix A) has been created in MATLAB/Simulink so as to investigate/calculate the prototype UPQC circuit waveforms, the dynamic and steady-state performance, and voltage and current ratings. Three typical case studies have been simulated and the results are presented below.

A three-phase three-wire UPQC connected to a weak supply point has been investigated. The 400 V three-phase three-wire system has the Thevenin impedance: $R = 0.04\,\Omega$ and $L = 0.4\,mH$. A nonlinear load (RL load connected to a rectifier) is supplied, which draws 5 kW and 5 kVAr. In addition, a linear load of 6 kW and 10 kVAr is supplied. On dc side a capacitor of 2000 μF is used. The interface inductors of both the shunt and series branches have the following parameters: L=1.245 mH and R=0.1 Ω. The filter capacitors used with the series and shunt branches are respectively 10 μF (connected in star) and 20 μF (connected in delta). A 4 Ω damping resistor is connected in series with the shunt filter capacitor. Coupling transformers are used to connect the series- and shunt active filters to the grid. The parameters of these transformers are given in Table 3.1. The

I_s^{ref} – reference source current magnitude;

$i_{s,a}^{ref}$, $i_{s,b}^{ref}$, $i_{s,c}^{ref}$ – reference source currents, respectively phase a, b and c;

$i_{s,a}$, $i_{s,b}$, $i_{s,c}$ – source currents, respectively phase a, b and c;

$v_{s,a}$, $v_{s,b}$, $v_{s,c}$ – source voltages, respectively phase a, b and c;

$\sin(\theta)$, $\sin(\theta-120)$, $\sin(\theta+120)$ – sine templates synchronized with the supply voltages, respectively phase a, b and c;

$\cos(\theta)$, $\cos(\theta-120)$, $\cos(\theta+120)$ – cosine templates synchronized with the supply voltages, respectively phase a, b and c;

V_L^{ref} – reference load voltage magnitude;

$v_{L,a}^{ref}$, $v_{L,b}^{ref}$, $v_{L,c}^{ref}$ – reference load voltages, respectively phase a, b and c;

ω – angular frequency;

C_{SH} – per-phase value of the shunt filter capacitance;

$V_L^{ref} \cdot \omega \cdot C_{SH}$ – magnitude of the fundamental current injected by the shunt filter capacitor;

$i_{cap,a}^{SH}$, $i_{cap,b}^{SH}$, $i_{cap,c}^{SH}$ – fundamental currents injected by the shunt filter capacitor, respectively phase a, b and c;

$v_{ind,a}^{SE}$, $v_{ind,b}^{SE}$, $v_{ind,c}^{SE}$ – voltage drop across the series filter inductor, respectively phase a, b and c;

R_{SE} – lumped resistance of the series filter inductor and series coupling transformer;

L_{SE} – lumped inductance of the series filter inductor and series coupling transformer.

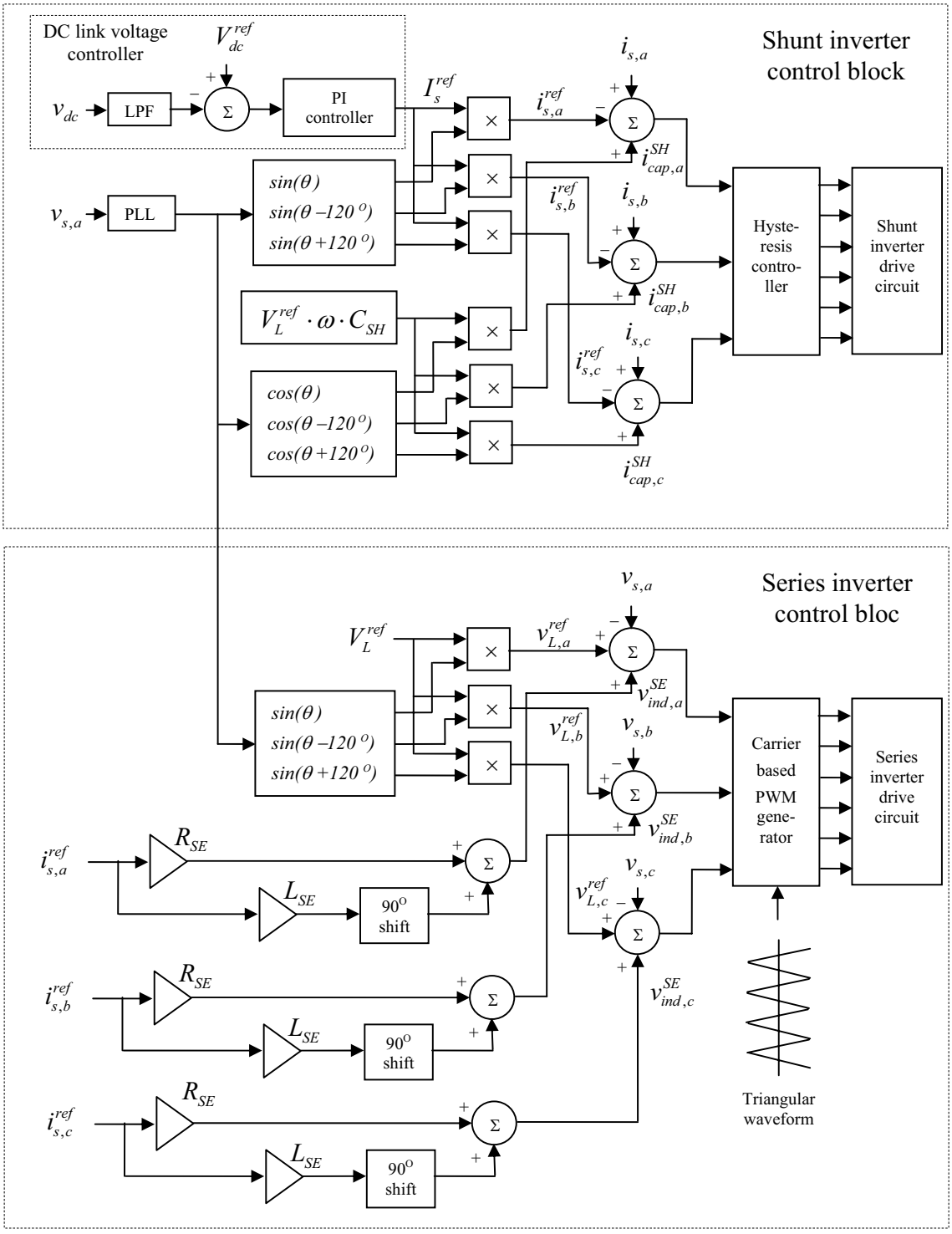


Fig.3.1.b. Block diagram of the UPQC overall control scheme

where v_l is the load voltage, v_t is the voltage at the PCC, and v_f is the voltage injected by the series filter.

In the case when the UPQC-P control strategy is applied, the injected voltage is in phase with the supply voltage; hence the load voltage is in phase with the supply voltage and there is no need for calculating the angle of the reference load voltage. Thus, the reference load voltage is determined by multiplying the reference magnitude (which is constant) with the sinusoidal template phase-locked to the supply voltage. Then, the reference series filter voltage is obtained using the expression (3.3.19).

Comparing the techniques for calculating the reference voltage of the series compensator, presented above, it can be concluded that the UPQC-P algorithm has the simplest implementation (it involves very little computation). In the UPQC-P case the voltage rating of the series compensator is considerably reduced. Also, the UPQC-Q compensation technique does not work in the case when the load is purely resistive. Therefore, the UPQC-P control strategy has been used in the UPQC simulation model (presented in section 3.4) and in the prototype UPQC (presented in section 3.5).

3.3.4. UPQC overall control scheme

Based on control strategies presented in subsections 3.3.1 – 3.3.3, the UPQC overall control scheme has been derived, which is shown in Fig.3.1.b, where:

v_{dc} – dc link voltage;

V_{dc}^{ref} – reference dc link voltage;

$$p = v_{a0} i_{a0} + v_{a2} i_{a1} + v_{a1} i_{a2} = v_{a1}^{*} i_{a1} + v_{a1} i_{a1}^{*} = 2\,\mathrm{Re}\left(v_{a1} i_{a1}^{*}\right) \tag{3.3.15}$$

Since the desired load voltages are balanced sinusoids and the currents flowing through the series compensator are also balanced (shunt compensator action), the instantaneous UPQC output power p_{out} is constant and this must be equal to the average power entering the UPQC (losses are neglected) $p_{in,av}$. Thus from (3.3.15) we get:

$$p_{out} = 2\,\mathrm{Re}\left(v_{l,a1} i_{s,a1}^{*}\right) = 2\left|v_{l,a1}\right|\left|i_{s,a1}\right|\cos\left(\theta_{vl,a1} - \theta_{is,a1}\right) = p_{in,av} \tag{3.3.16}$$

where $\theta_{vl,a1}$ and $\theta_{is,a1}$ are the angles of the vectors $v_{l,a1}$ and $i_{s,a1}$, respectively. From (3.3.16):

$$\theta_{vl,a1} = \cos\left(\frac{p_{in,av}}{2\left|v_{l,a1}\right|\left|i_{s,a1}\right|}\right)^{-1} + \theta_{is,a1} \tag{3.3.17}$$

The desired instantaneous symmetrical components of the load voltage are defined as:

$$\begin{bmatrix} v_{la0} \\ v_{la1} \\ v_{la2} \end{bmatrix} = \sqrt{\frac{3}{2}} \begin{bmatrix} 0 \\ V_m e^{j\theta_{vl,a1}} \\ V_m e^{-j\theta_{vl,a1}} \end{bmatrix} \tag{3.3.18}$$

Then the instantaneous load voltages are calculated by applying a transformation inverse to (3.3.14). Once the instantaneous load voltages are obtained, the reference series filter voltages are obtained using the following expression:

$$v_f = v_l - v_t \tag{3.3.19}$$

from the supply current. The quadratic equation (3.3.12) gives two solutions, from which the solution corresponding to a smaller voltage injection has to be chosen. The fundamental of the instantaneous injected voltage is obtained by multiplying $|V_f|$ determined from (3.3.12) with the sinusoidal template phase locked to the supply current. To compensate for supply voltage unbalance and distortion some additional component has to be added to the reference calculated above, which can be determined by subtracting the positive sequence fundamental component from the voltage at the PCC [50].

An alternative strategy for the determination of the UPQC-Q injected voltage reference, based on instantaneous symmetrical components, is proposed in [51]. The instantaneous power in a three-phase system is defined as:

$$p = v_a i_a + v_b i_b + v_c i_c \tag{3.3.13}$$

The instantaneous symmetrical components for i_a, i_b and i_c are defined as:

$$i_{a\,012} = \begin{bmatrix} i_{a0} \\ i_{a1} \\ i_{a2} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3.3.14}$$

where $a = e^{j120^o}$, and the subscripts 0, 1, and 2 correspond to zero, positive, and negative sequence respectively. For balanced currents the component $i_{a\,0}$ is equal to zero, and the component $i_{a\,1}$ is complex conjugate of $i_{a\,2}$. The same transformation is applied for voltages.

Taking into consideration (3.3.14) and above comments, equation (3.3.13) can be rewritten as:

series compensator is minimised and it also compensates for a part of the load reactive power demand. In UPQC-P case the series compensator does not compensate for any part of the reactive power demand of the load, and it has to be entirely compensated by the shunt compensator. Also the shunt compensator must provide the active power injected by the series compensator. Thus, in this case the VA rating of the shunt compensator increases, but that of the series compensator decreases. It can be concluded that the UPQC-Q and UPQC-P are two extreme cases and finding the optimum solution which is located in between is preferable. An analysis for optimisation of the converter rating is presented in [48-49] and an approximate sub-optimal control strategy for UPQC minimum losses operation is proposed.

An approach for generating the UPQC-Q reference voltage is presented in [50], which is based on the analysis of vector diagram for fundamental frequency. The load voltage $\overline{V}_l$ is equal to the sum of the voltage at the point of common coupling (PCC) $\overline{V}_t$ and the voltage injected by the series filter $\overline{V}_f$:

$$\overline{V}_l = \overline{V}_t + \left|V_f\right|(a + jb) \tag{3.3.11}$$

where $a + jb$ is a vector of unity magnitude and 90° ahead the supply current.

If the load voltage is assumed to be $\overline{V}_l = \left|V_l\right|\angle 0^o$ the following quadratic equation is obtained from (3.3.11):

$$\left|V_f\right|^2 - 2a\left|V_l\right|\left|V_f\right| + \left|V_l\right|^2 - \left|V_t\right|^2 = 0 \tag{3.3.12}$$

Solving this quadratic equation the magnitude of the injected voltage reference is obtained. As it was mentioned above, the phase of the injected voltage reference is 90°

In this work, because of its simple implementation and fast response, the preference is given to the PI controller. Thus, a PI controller has been used for dc link voltage control in the UPQC simulation model (presented in section 3.4) and in the prototype UPQC (presented in section 3.5). The dynamic performance of the dc link controller is improved using the adaptive control technique presented in section 6.3.

3.3.3. Control of the series active filter

The series component of UPQC is controlled to inject the appropriate voltage between the point of common coupling (PCC) and load, such that the load voltages become balanced, distortion free and have the desired magnitude. Theoretically the injected voltages can be of any arbitrary magnitude and angle. However, the power flow and device rating are important issues that have to be considered when determining the magnitude and the angle of the injected voltage [3]. Two UPQC terms are defined in [47] depending on the angle of the injected voltage: UPQC-Q and UPQC-P. In the first case (UPQC-Q) the injected voltage is maintained 90^{o} in advance with respect to the supply current, so that the series compensator consumes no active power in steady state. In second case (UPQC-P) the injected voltage is in phase with both the supply voltage and current, so that the series compensator consumes only the active power, which is delivered by the shunt compensator through the dc link. A detailed analysis of UPQC rating under different control strategies together with their advantages and disadvantages are presented in [47,77,78]. In the case of quadrature voltage injection (UPQC-Q) the series compensator requires additional capacity, while the shunt compensator VA rating is reduced as the active power consumption of the

active filter has to contain some amount of active current as compensating current. This active compensating current flowing through the shunt active filter regulates the dc capacitor voltage.

Usually a PI controller is used for determining the magnitude of this compensating current from the error between the average voltage across the dc capacitor and the reference voltage. In [22] a practical approach (Ziegler-Nichols tuning rules) for tuning the PI controller is proposed. The PI controller has a simple structure and fast response.

As an alternative to PI controller, a simple linear control technique is proposed in [23] with application to a single-phase shunt active filter. This is a proportional gain type control and the proportional coefficient is calculated instantaneously as a function of the dc capacitor average voltage error. Here, the expression used for calculation of the proportional coefficient is obtained through integration of a fist-order differential equation. However, the formula derivation for the proportional coefficient is not that simple for a three-phase UPQC, if possible at all (a high-order differential equation has to be integrated analytically). Also, a residual steady-state error occurs with a proportional only controller.

In [21,79,80], instead of the PI controller, a Fuzzy logic controller is proposed for processing the dc capacitor average voltage error. The Fuzzy controller is claimed to have some advantages over the PI controller: it does not require an accurate mathematical model, can work with imprecise inputs and handle non-linearity, and it is more robust. The simulation and experimental results presented in [21,79,80] show that the Fuzzy logic controller has a better dynamic behaviour than the PI controller. However, the steady-state performance of the Fuzzy controller is comparable to the PI controller.

of the hysteresis band. The controlled current is forced to decrease when it reaches the upper limit and to increase when it reaches the lower limit. By alternately reversing the polarity of the dc capacitor the controlled current is forced to alternately increase/decrease within the hysteresis band following the reference current. The narrower the hysteresis band (smaller values of h) the more accurate is the tracking, but this also results in higher switching frequency.

The hysteresis control method has simpler implementation, enhanced system stability, increased reliability and response speed [62]. However, this improvement is achieved on the penalty of wide range of variation in the switching frequency. Different modifications and improvements of hysteresis control in a constant frequency operation are proposed in [44-46], but these increase the complexity of the control circuit.

3.3.2. Voltage control of the dc bus

For a voltage source inverter the dc voltage needs to be maintained at a certain level to ensure the dc-ac power transfer. Because of the switching and other power losses inside UPQC, the voltage level of the dc capacitor will be reduced if it is not compensated. Thus, the dc link voltage control unit is meant to keep the average dc bus voltage constant and equal to a given reference value. The dc link voltage control is achieved by adjusting the small amount of real power absorbed by the shunt inverter. This small amount of real power is adjusted by changing the amplitude of the fundamental component of the reference current. The ac source provides some active current to recharge the dc capacitor. Thus, in addition to reactive and harmonic components, the reference current of the shunt

In [38] a modified Fourier method is proposed for reference current calculation, which employs a modified sliding-window Fourier computation approach using DSP. This computation method is claimed to be less time consuming than the conventional fast Fourier transform (FFT) and DFT algorithms. So, the controller response time can be reduced applying this computation method.

5) *Other techniques.*

The application of wavelet transform for the extraction of load current disturbance is proposed in [39-40]. A modified wavelet transform, termed the S-Transform is proposed in [41] for detecting, localising and classifying the power quality problems. Other digital filtering techniques discussed in detail in [43] can be used for extraction of the fundamental components.

Different current-control techniques are applied for tracking the reference current: sampled error control, hysteresis band control, sliding mode controller, linear quadratic regulator, deadbeat controller, pole shift controller [3]. From the number of dedicated papers, the *hysteresis control* appears to be the most preferable for shunt active filter applications. Therefore, in the UPQC simulation model (presented in section 3.4) and in the prototype UPQC (presented in section 3.5) a hysteresis controller has been used. The advantages of using a hysteresis controller are mentioned below.

In hysteresis control, the controlled current is monitored and is forced to track the reference within the hysteresis band (reference ± h). The inverter switches are made to change their states at instances when the controlled current touches the upper or lower limit

unbalanced and distorted supply voltages is presented in [33-34]. This approach also involves complex calculations and for its implementation a DSP is needed.

4) *Discrete Fourier transform (DFT).*

This is also a DSP-based control approach, which uses the well-known Fourier transformations for extracting the fundamental active/reactive components from the load currents. The samples of load currents are taken during one complete fundamental frequency cycle (or an integral number of cycles), and applying the DFT technique, the Fourier coefficients are calculated to identify the fundamental components of the load currents. The description of DFT algorithm is well documented in many references [35-36]. There are several performance limitations inherent in the application of DFT [36]:

- the waveform is assumed to be of a constant magnitude during the window size considered (stationary);
- the sampling frequency must be greater than twice the highest frequency of the signal to be analyzed, and
- the window length of data must be an exact integer multiple of power-frequency cycles.

Failing to satisfy these conditions will result in inaccurate waveform frequency analysis. Moreover, the DFT-based algorithm can lead to inaccurate results if the signal contains a dc component of decaying nature [37].

$$\begin{aligned} i_d &= \bar{i}_d + \tilde{i}_d \\ i_q &= \bar{i}_q + \tilde{i}_q \end{aligned} \tag{3.3.8}$$

The dc components $\bar{i}_d$ and $\bar{i}_q$ correspond to the fundamental load currents and the ac components $\tilde{i}_d$ and $\tilde{i}_q$ correspond to the load currents harmonics. Component $\bar{i}_q$ corresponds to the reactive power drawn by the load. The isolation of the ac component can be achieved by filtering out the dc offset. The compensation reference signals are obtained from the following expressions:

$$\begin{aligned} i_{d,ref} &= -\tilde{i}_d \\ i_{q,ref} &= -\bar{i}_q - \tilde{i}_q \end{aligned} \tag{3.3.9}$$

The shunt active filter reference currents in *a-b-c* frame are obtained with the following expression:

$$\begin{bmatrix} i^*_{f,a} \\ i^*_{f,b} \\ i^*_{f,c} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} i_{d,ref} \\ i_{q,ref} \end{bmatrix} \tag{3.3.10}$$

At first glance, this technique does not involve the source voltages in calculations, and the reference currents are derived directly from the load currents. So, it could seem that the calculation of reference currents using this approach is not affected by voltage unbalance or/and distortion. However, as it was mentioned above, a PLL is used with this technique, and the transformation angle is obtained from the supply voltage. So, the performance of this approach is also affected by the unbalance and distortion in supply voltages. A comparative analysis of this issue and above discussed control techniques under

calculations it is difficult to imagine its practical implementation without using a DSP. Some considerations on the development of DSP based shunt converters are given in [24]. The above-described technique for reference currents extraction only works when the supply voltages are balanced and harmonic free, as it was assumed above. As soon as the supply voltages become unbalanced or/and distorted, which is often the case in real power systems, the reference currents calculated with the expression (3.3.6) will result in poor compensation performance. One way of solving this problem is to extract the fundamental positive sequence voltages from the supply unbalanced or/and distorted voltages and use them in (3.3.6). This approach involves filtering, which requires even more calculations or additional hardware. Other approaches for reference currents extraction under unbalanced and/or distorted supply voltages are presented in [29-33].

3) Synchronous Reference Frame.

In this case the load currents presented in the $\alpha - \beta$ frame are transformed into a synchronous reference frame [34]:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{3.3.7}$$

The reference frame is synchronised with the supply voltage, and is rotating with the same frequency. A PLL is needed for implementing this method.

Like p and q in the instantaneous p-q approach presented above, i_d and i_q are also composed of dc and ac components:

currents. These two oscillating components are equal to zero if both the load currents and supply voltages are symmetrical and undistorted. In many cases the supply voltage asymmetry and distortion are so small that they can be neglected. So, the supply voltages are assumed to be symmetrical sinusoids. Then, if the load currents are symmetrical and undistorted, $\tilde{p} = 0$ and $\tilde{q} = 0$. When the load currents are either unsymmetrical or distorted $\tilde{p}$ and $\tilde{q}$ are different from zero and they have to be compensated by the shunt active filter.

In the case where the shunt active filter is to compensate for making the supply currents symmetrical, undistorted and in phase with the supply voltages, the shunt active filter reference currents in the $\alpha - \beta$ reference frame will be calculated as:

$$\begin{bmatrix} i_{f,\alpha}^{*} \\ i_{f,\beta}^{*} \end{bmatrix} = \frac{1}{v_{\alpha}^{2} + v_{\beta}^{2}} \begin{bmatrix} v_{\alpha} & -v_{\beta} \\ v_{\beta} & v_{\alpha} \end{bmatrix} \begin{bmatrix} \tilde{p} \\ \bar{q} + \tilde{q} \end{bmatrix} \tag{3.3.6}$$

The oscillating component $\tilde{p}$ is obtained by filtering out the constant component $\bar{p}$ from the total active power *p,* using a high-pass-filter (HPF). The expression similar to (3.3.3) is used to transform the currents from *α-β* to *a-b-c* reference frame. For the regulation of the dc capacitor voltage the active power loss compensative component p_{loss} has to be added to $\tilde{p}$ in (3.3.6) [28].

The instantaneous p-q theory and its application for reference currents calculation is discussed in detail in [3] and many supporting examples are presented. It is to be mentioned that when using this approach a Phase Lock Loop (PLL) is not needed. Being flexible and having a good dynamic response this approach has been addressed in many papers [26-30] with various interpretations and modifications. Since this approach involves complex

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{3.3.2}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{3.3.3}$$

The same transformation matrices are used for the transformation of currents.

Then from (3.3.1) the currents i_α and i_β are expressed:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \tag{3.3.4}$$

Both active p and reactive q powers defined above are composed of two components: constant (or dc) and oscillating.

$$\begin{aligned} p &= \bar{p} + \tilde{p} \\ q &= \bar{q} + \tilde{q} \end{aligned} \tag{3.3.5}$$

where $\bar{p}$ and $\bar{q}$ are the average active and reactive powers (dc values) originating from the symmetrical fundamental (positive sequence) component of the load current. $\bar{p}$ is the average active power delivered to the load, and $\bar{q}$ is the average reactive power drawn by the load. To improve the power factor, $\bar{q}$ has to be totally ($\cos\varphi = 1$) or partially ($\cos\varphi < 1$) compensated by the shunt active filter.

$\tilde{p}$ and $\tilde{q}$ are the ripple active and reactive powers (ac values) originating from the harmonic and asymmetrical fundamental (negative sequence) components of the load

To restore the average dc capacitor voltage to the reference level some active power has to be supplied to the dc capacitor, so the magnitude of the supply current has to be increased. When the average dc capacitor voltage increases, the magnitude of the supply current has to be decreased. So, by controlling the average voltage across the dc capacitor the amplitude of the supply current is automatically controlled. Applying this concept, the control circuit can by simplified and the number of current sensors reduced. Therefore, this control technique has been chosen to be used in the UPQC simulation model (presented in section 3.4) and in the prototype UPQC (presented in section 3.5). This approach is discussed in detail in [18-20]. The dc voltage regulation is achieved by using a proportional integral (PI) controller (the PI controller is used in many applications for its fast response and simple structure). The capacitor voltage is compared with some reference value and a PI controller processes the voltage error. The output of the PI controller is the magnitude of the reference supply current, and it is constant in steady-state. To get the source reference current, a sinusoidal template that is in phase with the supply voltage is multiplied by this magnitude.

2) *Instantaneous p-q theory*.

The concept of instantaneous active and reactive powers and its application for shunt active filter reference currents generation was introduced by Akagi et al. in [25]. The instantaneous active and reactive powers for a three-phase three-wire system are defined as:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{3.3.1}$$

where the three-phase voltages are transformed from *a-b-c* to *α-β* frame and vice versa using the following transformation relations:

waveform and phase of the supply current is known, only its amplitude needs to be determined. Also, when used with a hysteresis current controller, this control technique involves only the supply current measurement. Thus, this is a simpler to implement method. Therefore it has been used in the UPQC simulation model (presented in section 3.4) and in the prototype UPQC (presented in section 3.5)

The current reference circuit generates the reference currents required to compensate the load current harmonics and reactive power, and also maintain the dc link voltage constant. There are many possibilities to implement this type of control, and the most popular of them will be presented in the following.

1) *Average dc voltage regulation.*

This approach is used for supply reference current determination and it is based on the fact that the magnitude of the supply current depends on power balance between the supply and the load. The dc capacitor serves as energy storage element. If the shunt active filter losses are neglected, in steady-state, the power supplied by the system has to be equal to the real power demand of the load, and no real power flows into the dc capacitor. The average dc capacitor voltage is thus maintained at reference voltage level. If a power unbalance caused by a load change occurs, the dc capacitor must supply the power difference between the supply and load that will result in reducing the dc capacitor voltage.

3.3. Control strategy

3.3.1. Control of the shunt active filter

The effectiveness of an active power filter depends basically on the design characteristics of the current controller, the method implemented to generate the reference template and the modulation technique used. The control scheme of a shunt active power filter must calculate the current reference waveform for each phase of the inverter, maintain the dc voltage constant, and generate the inverter gating signals. Also the compensation effectiveness of an active power filter depends on its ability to follow the reference signal calculated to compensate the distorted load current with a minimum error and time delay.

The shunt component of UPQC can be controlled in two ways:

- *Tracking the shunt converter reference current*, when the shunt converter current is used as feedback control variable. The load current is sensed and the shunt compensator reference current is calculated from it. The reference current is determined by calculating the active fundamental component of the load current and subtracting it from the load current. This control technique involves both the shunt active filter and load current measurements.

- *Tracking the supply current*, when the supply current is used as the feedback variable. In this case the shunt active filter ensures that the supply reference current is tracked. Thus, the supply reference current is calculated rather than the current injected by the shunt active filter. The supply current is often required to be sinusoidal and in phase with the supply voltage. Since the

the *di/dt* of the harmonic component of the load, so that the proper harmonic cancellation can take place. On one hand, for a better harmonic cancellation and reactive power compensation a higher inductance is preferable, but on the other hand, too high inductance will result in slow dynamic response of the shunt compensator and it could not be possible to compensate for some of the load harmonics. So, a compromise solution has to be found. A higher dc link reference voltage results in a higher *di/dt* of the shunt compensator, better dynamic response and reactive power compensation performance, but it also increases the stress experienced by the inverter switching devices. Again, a compromise solution has to be adopted. The dc capacitor size is selected to restrict the dc voltage ripple within reasonable limits. The dc voltage ripple is determined by both the amount of reactive power to be compensated and the active power supplied by dc capacitor during the transient.

To correct for the effects of supply voltage distortion, the series compensator is required to inject appropriate harmonic voltages. This unfortunately can present problems with unbalanced fluxes if conventional three-limb injection transformers are used. To avoid this, three separate injection transformers are utilized. This allows the flux-linkage in each to be dealt with separately and remains true regardless of the external configuration, star, or delta.

- The shunt compensator in the right-shunt configuration can supply the entire load reactive power requirement, whereas in the case of the left-shunt UPQC the shunt compensator can only partially supply the load reactive power;
- It has been shown that the dc capacitor control of the right-shunt UPQC structure is simpler;
- Overall the characteristics of the right-shunt UPQC are superior to those of the left-shunt UPQC.

Thus, it can be concluded that the right-shunt UPQC is more advantageous. Therefore this configuration has been used in the UPQC simulation model (presented in section 3.4) and in the prototype UPQC (presented in section 3.5)

3.2. Power circuit design considerations

The design of UPQC power circuit includes the selection of the following three main parameters:

- shunt interface inductors;
- dc link reference voltage;
- dc link capacitor.

Design recommendations on selection of the above three parameters are presented in [19, 21, 52, 62]. The design of the shunt interface inductor and the dc reference voltage is based on the following criteria. Limiting the high frequency components of the injected currents; the instantaneous *di/dt* generated by the shunt active filter should be greater than

injected voltage of desired magnitude, waveform, phase shift and frequency, the desired signal is compared with a triangular waveform signal of higher frequency, and appropriate switching signals are generated. The dc capacitor is alternately connected to the inverter outputs with positive and negative polarity. The output voltages of the series VSI do not have the shape of the desired signals, but contain switching harmonics, which are filtered out by the series low pass filter. The amplitude, phase shift, frequency and harmonic content of injected voltages are controllable.

Two possible ways of connecting the UPQC to the point of common coupling (PCC) are discussed in [3]:

- Right-shunt UPQC compensation configuration: The shunt component is connected to the load side and the series to the supply side;
- Left-shunt UPQC compensation configuration: The shunt component is connected to the supply side and the series component to the load side.

Also, their control and characteristics are presented for both compensation configurations. Comparing the characteristics of these two configurations the following conclusions are made [3]:

- The right-shunt UPQC can operate in zero power injection/absorption mode, whereas the left-shunt cannot;
- The right-shunt UPQC can make the power factor unity at the load terminal, whereas for the left-shunt UPQC the power factor at the load terminal depends on the load;

the reference current is tracked. This control technique is called “hysteresis band control” [3].

The dc side capacitor serves two main purposes: it maintains the dc voltage with a small ripple in the steady state, and it serves as an energy storage element to supply a real power difference between the load and source during the transient period [21]. The average voltage across the dc capacitor is maintained constant, and in order that the shunt active filter can draw a leading current, this voltage has to be higher then the peak of the supply voltage. This is achieved through an appropriate proportional-integral (PI) control, by regulating the amount of active current drawn by the shunt active filter from the system.

The series active filter is responsible for voltage compensation during supply side disturbances, such as voltage sag/swell, flicker and unbalance. The series part of the UPQC also consists of a VSI connected on the dc side to the same energy storage capacitor, and on the ac side it is connected in series with the feeder, through the series low pass filter (LPF) and coupling transformers. The series LPF prevents the switching frequency harmonics produced by the series VSI entering the system. The series coupling transformers provide voltage matching and isolation between the network and the VSI.

The series active filter compensation goals are achieved by injecting voltages in series with the supply voltages such that the load voltages are balanced and undistorted, and their magnitudes are maintained at the desired level. This voltage injection is provided by the dc storage capacitor and the series VSI. Based on measured supply and/or load voltages the control scheme generates the appropriate switching signals for the series VSI switches. The series VSI is controlled in voltage-control mode using the well-known pulse-width-modulated (PWM) switching technique described in detail in [17]. In order to produce the

The shunt active filter is responsible for power factor correction and compensation of load current harmonics and unbalances. Also, it maintains constant average voltage across the DC storage capacitor. The shunt part of the UPQC consists of a VSI (voltage source inverter) connected to the common DC storage capacitor on the dc side and on the ac side it is connected in parallel with the load through the shunt interface inductor and shunt coupling transformer. The shunt interface inductor, together with the shunt filter capacitor are used to filter out the switching frequency harmonics produced by the shunt VSI. The shunt coupling transformer is used for matching the network and VSI voltages.

In order to achieve its compensation goals, the shunt active filter injects currents at the point of common coupling such that the reactive and harmonic components of the load currents are cancelled and the load current unbalance is eliminated. This current injection is provided by the dc storage capacitor and the shunt VSI. Based on measured currents and voltages the control scheme generates the appropriate switching signals for the shunt VSI switches. The particular currents and voltages to be measured depend on the applied control strategy. The shunt VSI is controlled in current control mode. The appropriate VSI switches are turned on and off at certain time instances such that the currents injected by the shunt active filter track some reference currents within a fixed hysteresis band (assuming a hysteresis controller is used) according to the compensation objectives. The VSI switches alternately connect the dc capacitor to the system, either in the positive or negative sense. When the dc capacitor voltage is connected in the positive sense, it is added to the supply voltage and the VSI current is increasing. In the case of the dc capacitor connected in the negative sense, its voltage is in opposition to the supply voltage and the VSI current is decreasing. So, alternately increasing and decreasing the current within the hysteresis band,

Chapter 3

UNIFIED POWER QUALITY CONDITIONER - UPQC

3.1. Power circuit structure and principle of operation

The UPQC is a combination of series and parallel active power filters connected back-to-back to a common dc energy storage capacitor, as mentioned earlier. One form of UPQC structure, which is used in three-phase three-wire systems, is shown in Fig.3.1.a. Other UPQC structures, including tree-phase four-wire systems, are discussed in [3].

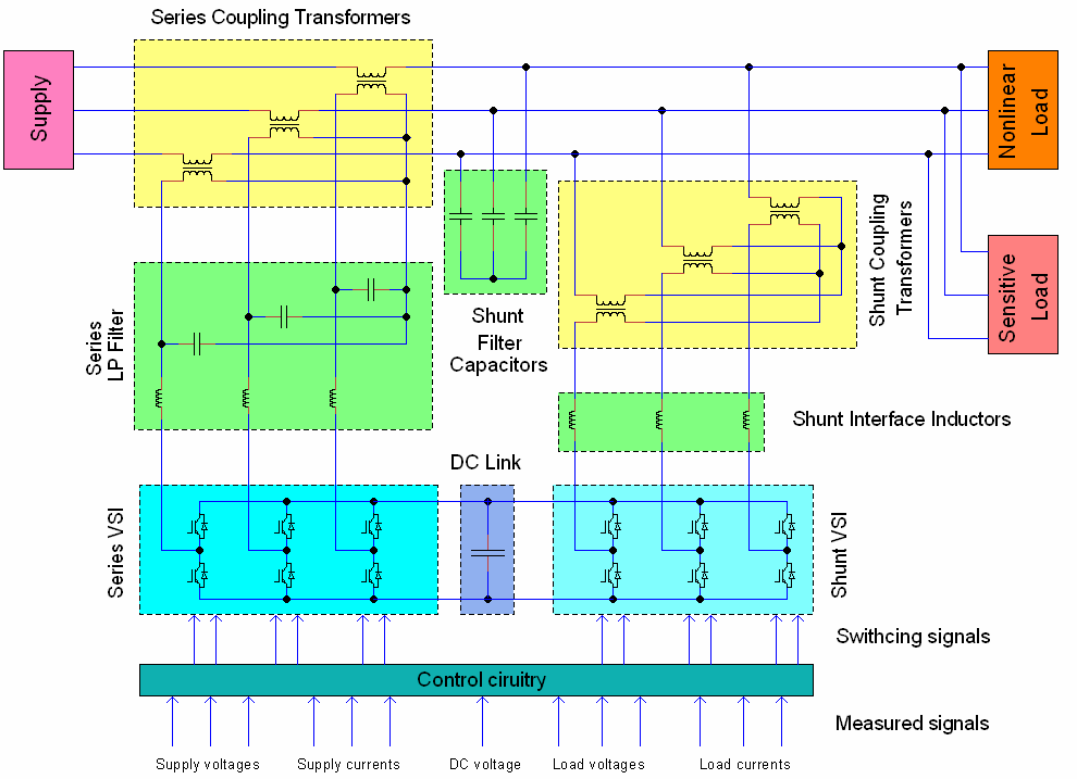


Fig.3.1.a. Power circuit diagram of a three-phase UPQC

UPQC is much more flexible than separately configured DSTATCOM and DVR. However it is an expensive device and its use may be limited to particular sensitive situations with a high value on power quality [3]. More research is necessary to investigate its full capability and minimize the cost. Also for the purpose of cost justification new applications of UPQC must be explored. The present work focuses on this promising device – UPQC. In the next chapter the power circuit configuration, operating principles and control strategy of UPQC are discussed.

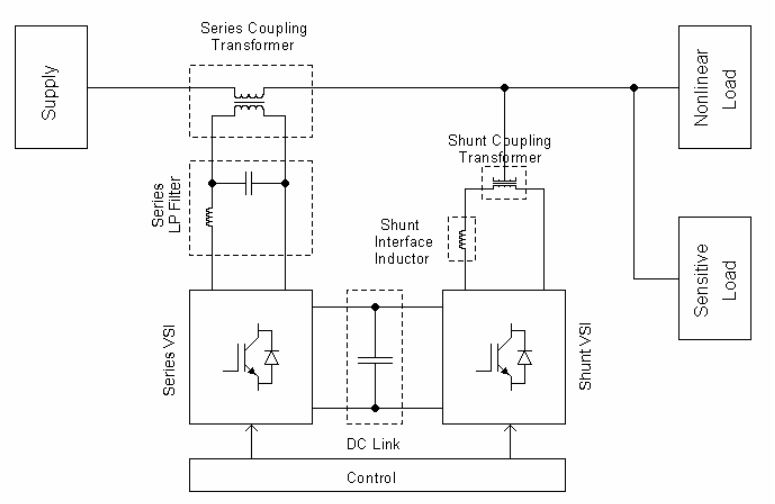


Fig.2.3. System configuration of UPQC

The shunt component is responsible for mitigating the power quality problems caused by the consumer: poor power factor, load harmonic currents, load unbalance, DC offset. It injects currents in the ac system such that the source currents become balanced sinusoids and in phase with the source voltages. The shunt device is also used for providing a path for real power flow to aid the operation of the series connected VSI. It can be concluded here that a UPQC combines together the operation of two previously discussed custom power devices: DVR and DSTACOM.

The main advantage of UPQC is that it does not require any energy storage [2]. It can be designed to mitigate any sag above a certain magnitude, independent of its duration. This could result in a device that is able to compete with the uninterruptible power supply (UPS) typically used for the protection of low-power, low-voltage equipment. The main disadvantage of UPQC is the large current rating required to mitigate deep sags. For low-power, low-voltage equipment this will not be a serious concern, but it might limit the number of large power and medium-voltage applications.

fundamental and pure resistance for the harmonics. Thus, a small-rated active filter improves the characteristics and eliminates the drawbacks of high-rated passive filter.

In [70] and [62] a shunt hybrid filter consisting of a small-rated active filter connected in series with a passive filter is proposed. This hybrid filter is connected in parallel with the load. The active filter is controlled in such a way as to behave as a negative or positive resistor. The negative resistance presented by the active filter cancels the positive resistance inherent in the passive filter, so that the hybrid filter acts as an ideal passive filter with infinity quality factor. This significantly improves damping of harmonic resonance, compared with the passive filter on its own. When the active filter acts as a positive resistor the flowing of excessive harmonic current through the passive filter is prevented.

2.2.5. Unified power quality conditioner - UPQC

The UPQC is a custom power device that integrates the series- and shunt active filters, connected back-to-back on the dc side and sharing a common DC capacitor [14], as shown in Fig.2.3. It employs two voltage source inverters (VSIs) that are connected to a common DC energy storage capacitor. One of these two VSIs is connected in series with the feeder and the other is connected in parallel to the same feeder.

The series component of the UPQC is responsible for mitigation of the supply side disturbances: voltage sags/swells, flicker, voltage unbalance and harmonics. It inserts voltages so as to maintain the load voltages at a desired level; balanced and distortion free.

devices, particularly those installed upstream. Impacts on the system and on customers when applying a DVR and its protection issues are discussed in [15].

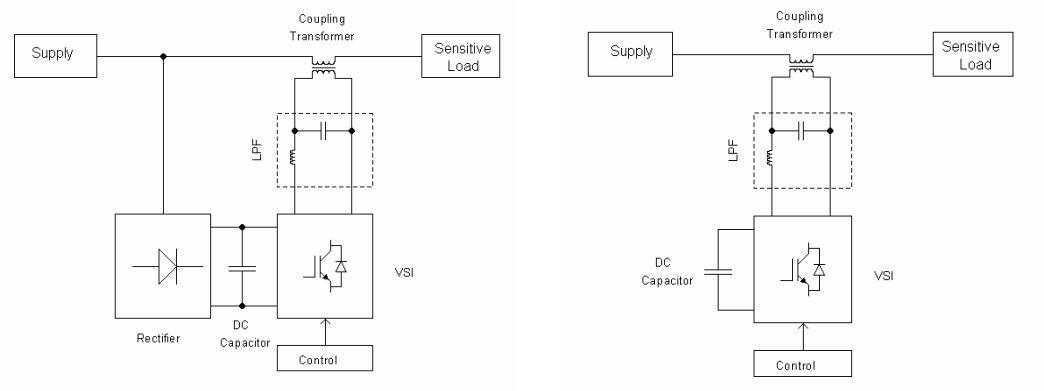
Since the DVR is one of the two components forming UPQC, its power circuit and control aspects are further discussed in the next chapter where the UPQC is presented in detail.

2.2.4. Hybrid filters

In section 2.1.6 the drawbacks of passive filters have been mentioned. Thus, despite their simplicity, low cost and high efficiency, the passive filters have many problems to discourage their application. Also, the pure active power filters discussed in sections 2.2.2 and 2.2.3 have some problems and are not always cost-effective solutions, especially at large kVA ratings [67]. Hybrid filter topologies consist of both active and passive filters in different configurations [69]. They effectively address and mitigate the problems of both passive filter and pure active filter solutions, and provide a cost-effective and practical harmonic compensation approach, particularly for high power non-linear loads. Thus, hybrid topologies improve significantly the compensation characteristics of simple passive filters, making the use of active power filter available for high power applications, at a relatively lower cost [62].

A combined system of shunt passive filter and small-rated series active filter is proposed in [67-69] and [71]. The series active filter acts as an active impedance, which prevents resonances in the shunt passive filter and improves its filtering characteristics. The series active filter is controlled in such a way as to present zero impedance for the

network. DVR structures, control techniques and rating requirements are discussed in detail in [3].



(a) Rectifier supported DVR (b) DC capacitor supported DVR

Fig.2.2. Two possible system configurations of DVR

The DVR coupling transformer can experience saturation during the transient period after a voltage sag starts. For preventing this, normally a rating flux that is double of the steady-state limit is chosen. An alternative method for preventing the coupling transformer saturation, which consists in limiting the flux-linkage during the transient switch-on period, is proposed in [12].

The DVR coupling transformer performs two important functions: voltage boost and electrical isolation. However, it increases the DVR costs, requires space, contributes to DVR losses, and as mentioned above can be driven into saturation in some conditions. In [13] and [16] a DVR structure without a coupling transformer is proposed.

The DVR acts as an additional energy source and introducing it into the system has effects seen both by system and customer. So, when applying a series device, careful considerations must be taken. For example, the DVR must coordinate with other protective

one of the two components forming UPQC, its power circuit and control aspects are further discussed in the next chapter where the UPQC is presented in detail.

2.2.3. Dynamic voltage restorer - DVR

DVR is a series-connected custom power device the aim of which is to protect sensitive loads from supply side disturbances except outages. Also, the DVR can act as a series active filter, isolating the source from harmonics generated by loads. The DVR consists of a voltage-source PWM converter equipped with a dc capacitor and connected in series with the utility supply voltage through a low pass filter (LPF) and a coupling transformer [11]. Typical circuits are shown in Fig.2.2. This device injects a set of controllable three-phase ac voltages in series and synchronism with the distribution feeder voltages such that the load-side voltage is restored to the desired amplitude and waveform even when the source voltage is unbalanced or distorted. There are two different DVR structures [3]: a rectifier supported DVR, Fig.2.2(a), and a capacitor supported DVR, Fig.2.2(b). The first one can absorb real power from the grid through a rectifier. This is not possible with the capacitor supported DVR, and therefore in the steady state it has to be operated in “no real power” exchange mode. In [76] a DVR structure utilising batteries for energy storage is investigated. In this case, the real power required for voltage sag compensation is drawn from the batteries connected across the dc link. The DVR cannot mitigate any interruptions, and unless it is rectifier supported it cannot mitigate very deep sags [2]. The rectifier supported DVR injects current harmonics into the distribution

Weighing the pros in cons of voltage- and current-source inverters, it can be concluded that the voltage-source inverter is preferable to the current-source inverter.

The shunt active power filter operates as a current source and compensates current harmonics by injecting the harmonic components generated by the load but phase shifted by 180 degrees [62]. Moreover, with an appropriate control scheme, the shunt active power filter can also compensate for the load power factor. As a result, components of harmonic currents contained in the load current are cancelled by the effect of the active filter, and the source current remains sinusoidal and in phase with the respective phase-to neutral voltage. Thus, ideally a three-phase shunt active filter injects a set of three-phase currents such that the source currents become in phase with the source voltages, are DC offset and harmonic free, and are balanced. Also, the shunt active power filter has the capability of damping harmonic resonance between an existing passive filter and the supply impedance [9].

The use of two or more PWM voltage source inverters (VSIs) connected in cascade is an interesting alternative to compensate high power nonlinear loads [65]. Connecting in cascade two VSIs with different rated power allows the use of different switching frequencies, reducing switching stresses, and commutation losses in the overall compensation system. Of these two VSIs, one compensates for the reactive power demand and lower frequency current harmonics, while the other one compensates only high-frequency current harmonics. The first converter requires higher rated power than the second and can operate at lower switching frequency.

A quite detailed discussion of DSTATCOM structure, control and practical aspects is given in [3], [62] and many other relevant publications. Since the shunt active power filer is

Use of the current-source PWM converter (a dc inductor serves as storage element) is also possible, but the voltage-source PWM converter has a higher efficiency, lower cost, smaller physical size and other advantages [9-10]. Also, the current-source PWM converter cannot be used in multilevel or multistep mode configurations to allow compensation in higher power ratings [62, p.1068]. A comparative analysis of voltage-source and current-source shunt active power filters is presented in [64]. The pros and cons of both voltage- and current-source inverters are summarised in Table 2.4 below.

Table 2.4. Advantages and disadvantages of voltage-source and current-source inverters

Inverter type	Advantages	Disadvantages
Voltage-source	– High efficiency near the nominal operating point; – Lower cost; – Smaller physical size; – Expandable to multilevel and multistep versions, to improve its performance for high power ratings.	– Low efficiency when the load power is low; – Limited lifetime of the electrolytic capacitor.
Current-source	– Simple open loop current control is possible; – High efficiency when the load power is low.	– Bulky and heavy dc inductor; – Requires higher values of parallel capacitor filters at the ac terminals to remove unwanted current harmonics; – A separate clamp circuit is needed to protect the switching devices against overvoltages; – High dc link losses; – Low efficiency near the nominal operating point; – Cannot be used in multilevel or multistep configurations, to allow compensation in higher power ratings.

2.2.2. Distribution static compensator - DSTATCOM

DSTATCOM is a shunt-connected custom power device the primary aims of which are [3]:

- power factor correction;
- current harmonics filtering;
- load DC offset cancellation;
- load balancing;

It can also be used for voltage regulation at a distribution bus.

Being an active filtering device connected in shunt with the harmonic-producing load, DSTATCOM is often referred as shunt or parallel active power filter. DSTATCOM consists of a voltage-source PWM converter equipped with a dc capacitor as storage element, interface inductor and if necessary a matching transformer, Fig.2.1.

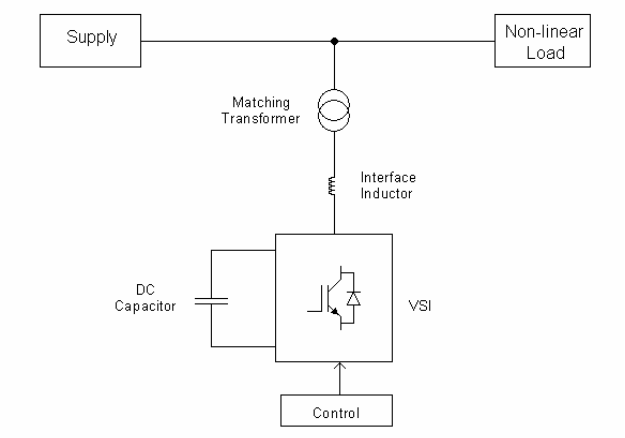


Fig.2.1. System configuration of DSTATCOM

combination of GTO and thyristor switches, which can interrupt a fault current and can also perform auto-reclosing function.

Additionally the *solid state fault-current limiter* (SSCL) has been proposed [7], which significantly reduces the fault-current magnitude within one or two cycles. This is a GTO based device that inserts a limiting inductor in series with the faulted circuit as soon as the fault is detected. After fault clearing the inductor is removed from the circuit.

Before connecting a SSCL or SSCB in a distribution network two important issues have to be considered:

- The identification of locations in the network in which such devices can be placed.
- The coordination of the protective devices. A limiter or breaker placed in a network must not adversely affect the downstream protective devices.

The sensitive loads are usually connected to two incoming feeders through a load transfer switch. At any given time the load is supplied by one of the two feeders. In case of a severe voltage sag/swell or interruption in the supplying feeder the *solid state transfer switch* (SSTS) quickly transfers the load to a healthy feeder [8]. This is usually a thyristor-based device that can perform a sub-cycle load transfer. It can also be used as a bus coupler between two incoming feeders.

The above-mentioned devices belong to the family of so-called network reconfiguring devices. Their topology, principle of operation, control, application and practical limitations are discussed in detail in [3].

2. 2. Overview of major custom power devices

In 1995, N.G. Hingorani introduced the Custom Power (CP) concept in [4]. Custom Power embraces a family of power electronic devices, or a toolbox, which is applicable to distribution systems to provide power quality solutions. This technology has been made possible due to the widespread availability of cost effective high power semiconductor devices such as gate turn off (GTO) thyristors and Insulated gate bipolar transistors (IGBTs), low cost microprocessors and techniques developed in the area of power electronics. In this section, an overview of major CP devices is presented.

2.2.1. Network reconfiguring devices

A short-circuit fault always causes a voltage sag for some costumers. The severity of the voltage sag depends on fault current magnitude and duration. To reduce the severity of the voltage sag one has to reduce the fault-clearing time or/and to reduce the magnitude of the fault current.

A considerable reduction in fault clearing time is achieved by using *current-limiting fuses* [5], which are able to clear a fault within half a cycle, so that the duration of a voltage sag will rarely exceed one cycle. However, because of the fuse element melting during the fault, this device needs human intervention for replacement after the fault clearance.

The *solid state circuit breaker* (SSCB) [6] is a multi-operation device, which also provides a fault clearing time within one half-cycle. This is a device, based on a

Power electronic controllers provide a flexible choice and a better performance to alleviate the power quality problems. These modern power electronic based systems are called *custom power devices* [3]. There are many custom power devices and they are divided in two groups: network-reconfiguring type and compensating type. The network-reconfiguring group includes the following devices: solid-state current limiter (SSCL), solid-state breaker (SSB) and solid-state transfer switch (SSTS). These devices are much faster than their mechanical counterparts. The compensating devices either compensate a load, correcting its power factor, unbalance etc., or improve the quality of the supply voltage. These devices are either connected in shunt or in series or a combination of both. The compensating group includes: distribution static compensator (DSTATCOM) to compensate for load reactive power and current harmonics, dynamic voltage restorer (DVR) for voltage support, and unified power quality conditioner (UPQC) for both current and voltage compensation. The present work focuses on the last custom power device – UPQC, which is a combination of a shunt and series device and can combine the functions of these two devices together. An overview of the major custom power devices mentioned above is presented in the next section.

created that is worse than the condition being corrected. The filtering characteristics of the shunt passive filter are strongly influenced by the source impedance, which is not accurately known and varies with the system configuration [66]. Transformer connections employing phase shift are sometimes used for cancellation of triplen (3^{rd}, 9^{th}, 15^{th}, etc.), 5^{th} and 7^{th} harmonic currents. Both passive filters and transformer connection have a disadvantage that they cannot respond to changing load and harmonic conditions. Moreover, the use of passive elements at high power level makes these devices bulky. Conventionally, the power factor correction is performed by means of capacitor banks, synchronous condenser and static VAR compensators (SVCs). Harmonic resonance problems are sometimes found with the use of passive capacitor banks. Using the synchronous condenser the resonance problems are eliminated, but they are expensive and their operation and maintenance are more costly. Both capacitor banks and synchronous condenser have a slow response. SVCs generate a considerable amount of harmonics that may have to be filtered. Also, due to their high cost, the SVCs are not economical for small power users. Tap-switching and ferro-resonant voltage regulators were the only devices to compensate for undervoltages and overvoltages. However, it was not possible to compensate for short duration sags because the fast control devices were not available. The conventional mitigation techniques are discussed in detail in [1-3], highlighting their deficiencies.

It must be appreciated that the above-discussed conventional techniques are not flexible enough. Therefore it is imperative that better and flexible mitigating devices are used for power quality problems. The implementation of such devises has become possible due to advances in power electronics and availability of fast acting controllers like DSP.

Improving the load equipment immunity to disturbances and adding appropriate correcting devices and control so that the equipment does not draw reactive and harmonic currents from the utility are solutions applicable only to new equipment, and hence they are local solutions [47]. These solutions cannot solve the problem of polluting and sensitive load equipments that already exist, and their replacement and redesign are not always economically feasible. Also, incorporating additional modules that will improve the power factor and compensate for harmonic currents in very small equipment can considerably increase their overall cost and may not be a viable solution for customers. However, the power quality considerations should be kept in mind while designing new equipment. Considering these drawbacks of local solutions, other more global strategies have to be applied. Power quality of an entire plant or a group of customers can be improved by inserting the independent compensating devices at the point of utility-customer interface or other relevant points in the distribution grid. In this case the necessity of designing the individual equipments in conformity with power quality standards can be relaxed, and the polluting equipment that already existed is not a problem.

Power quality problems are as old as power distribution through feeders, and the partial mitigation of these problems existed even before the advent of power electronic controllers [61]. These are so called conventional mitigation techniques. For example, to compensate for the load current harmonics, passive filters based on inductors and capacitors were used and are still used in many power transmission and distribution applications. However, applying passive harmonic filters requires careful consideration. Series-tuned filters present a low impedance to harmonic currents, but they also form a parallel resonance circuit with the source impedance. In some instances, a situation can be

- equipment has become more sensitive to voltage disturbances;
- some equipment causes voltage disturbances;
- a growing need for standardization and performance criteria;
- in order to be competitive utilities want to deliver a good product;
- power quality can be measured.

Details on each of these reasons can be found in [2].

In addition, deregulation in the power industry have has had an impact on power quality issues [42]. In the new electricity markets the power quality is treated as a commodity that can be traded and this has added a new dimension to the power quality.

2.1.6. Solution strategies and mitigating techniques

The power quality problems can be viewed as the difference between the quality of power supplied and the quality of the power required for reliable operation of the load equipment. Using this viewpoint, the power quality problems can be resolved in one of three ways:

- reducing the power supply disturbances;
- improving the load equipment immunity to disturbances;
- inserting some mitigating equipment between the electrical supply and the sensitive loads.

Practicality and economics determine the extent to which any of these options can be used in a particular case. The present work focuses on the third option.

2.1.5. Importance of quality power

Due to the proliferation of electronics, electrical devices are becoming smaller and more sensitive to power quality aberrations. For example, an electronic controller about the size of a shoebox can efficiently control the performance of a 750 kW motor; while the motor might be somewhat immune to power quality problems, the controller is not. The load equipment of the latest generation, with microprocessor-based controls and power electronic devices, is more sensitive to power quality disturbances than the equipment previously used. Also, many things are now interconnected in a network. Integrated processes mean that the failure of any component has much more important consequences. In some instances electrical equipment causes its own power quality problems.

The increasing emphasis on overall power system efficiency has resulted in continued growth in the application of devices such as high-efficiency, adjustable-speed motor drives and shunt capacitors for power factor correction to reduce losses [61]. This has resulted in an increase in the harmonic content of the power systems and has concerned many people about the future impact on system capabilities.

Nowadays, the users of electrical power are quite aware of power quality issues. More and more electricity customers are becoming better informed about such power quality issues as interruptions, sags, and switching transients. Thus, the utilities are challenged by customers to improve the quality of the power delivered.

Both electric utilities and end users of electric power are increasingly concerned about the quality of electric power. The recent increased interest in power quality is mainly as a result of the following concerns:

2.1.4. Power quality monitoring

Generally, the causes of power quality problems are complex and difficult to detect. To be able to solve power quality problems comprehensive knowledge of power quality issues is necessary. Two ways of obtaining information about the power quality are identified: monitoring and stochastic prediction [2]. Monitoring is still the method most commonly used, but the trust in prediction techniques is likely to grow.

The only way of getting an accurate picture of power quality is still by means of measuring. Solving power quality problems depends on obtaining meaningful data at the optimum location or locations and within an appropriate time frame. In order to acquire useful and relevant data, instruments most suited for a particular application should be utilised. Using inappropriate or inadequate instruments can result in unrecognised power quality problems. Some of the commonly used power quality instruments are discussed in [1], together with their area of application.

The following steps are very important when solving the power quality problems:

- the determination of test location or locations;
- number of test locations;
- test duration, instrument setup.

Discussions and guidelines on these steps are given in [1].

In Table 2.2 [62] the harmonic voltage limits that are recommended for utility companies by IEEE Standard 519-1992 are given. The harmonic voltage limits according to EN 50160 Standard are given in Table 2.3 [63].

Table 2.2. Voltage distortion limits (IEEE Standard 519-1992)

Bus voltage at PCC	Individual harmonic magnitude (%)	Total voltage distortion (THD in %)
≤ 69 kV	3.0	5.0
69.001 – 161 kV	1.5	2.5
> 161 kV	1.0	1.5

Table 2.3. Values of individual harmonic voltages at the supply terminal for orders up to 25, given in percent of U_n (EN 50160 Standard)

Odd harmonics				Even harmonics	
Not multiples of 3		Multiples of 3			
Order *h*	Relative voltage (%)	Order *h*	Relative voltage (%)	Order *h*	Relative voltage (%)
5	6.0	3	5.0	2	2.0
7	5.0	9	1.5	4	1.0
11	3.5	15	0.5	6 … 24	0.5
13	3.0	21	0.5		
17	2.0				
19	1.5				
23	1.5				
25	1.5				

these many standards, the following two will be further referred when appropriate and are highlighted here:

- EN 50160, "*Voltage Characteristics of Public Distribution Systems"*;
- IEEE Standard 519-1992, "*IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems"*.

A critical review of various standards is given in [2], including the detailed description of the European voltage characteristic standard, EN 50160. Some standards are still under development and even more standards are required to fully standardize equipment as far as power quality is concerned. Proper standardization has to solve the problem of responsibility for power quality disturbances.

Table 2.1 [62] shows the harmonic current limits in IEEE Standard 519-1992 for general distribution systems, 120 V – 69 kV.

Table 2.1. Current distortion limits for general distribution systems, 120 V – 69 kV (IEEE Standard 519-1992)

Maximum harmonic current distortion in percent of I_L						
I_{SC}/I_L	<11	$11 \le h < 17$	$17 \le h < 23$	$23 \le h < 35$	$h \ge 35$	*THD*
< 20[1]	4.0	2.0	1.5	0.6	0.3	5.0
$20 < 50$	7.0	3.5	2.5	1.0	0.5	8.0
$50 < 100$	10.0	4.5	4.0	1.5	0.7	12.0
$100 < 1000$	12.0	5.5	5.0	2.0	1.0	15.0
≥1000	15.0	7.0	6.0	2.5	1.4	50.0

Individual harmonic order *h* (odd harmonics).
Even harmonics are limited to 25% of the odd harmonic limits above.
Current distortions that result in a dc offset are not allowed.
[1] All power generation equipment is limited to these values of current distortion regardless of the value of I_{SC}/I_L.

quality. The voltage quality (for which the network is often considered responsible) and current quality (for which the customer is often considered responsible) affect each other by mutual interaction. Thus, both suppliers and consumers of electricity are responsible for maintaining the power quality parameters within the standards limits. The particular responsibilities of the suppliers and users of electric power are discussed in [1]. Suppliers are mostly responsible for continuity of supply and for maintaining the voltage magnitude in different points of the distribution grid within the prescribed limits. The consumers should be responsible for energy conservation, harmonic current injection, power factor, and surge current demand.

2.1.3. Power quality standards

Power quality mitigation methods require technical solutions, which can be implemented independently of any standardization. But proper standardization provides important incentives for the implementation of the technical solutions. That is why standards that define the quality of power supply have been in existence for decades. The power quality standards are mostly concerned with the following three areas [2]:

- defining the nominal environment,
- defining the terminology;
- limiting the number of power quality problems.

The International Electrotechnical Commission (IEC) and the Institute of Electrical and Electronics Engineers (IEEE) have proposed their sets of power quality standards. Of

Due to the presence of unbalanced loads, voltages become unbalanced, and negative and zero sequence voltages are generated, which if applied to an induction motor may give rise to extra losses and sometimes torque pulsation and reduction. Together, these effects can contribute to overloading of an induction motor.

Various forms of disturbances in supply voltage such as interruption, distortion, overvoltage/undervoltage, sag/swell, flicker etc. can occur in power systems. These can have serious consequences for consumers. For example, the complete stopping of a process line can be caused by relay tripping due to a voltage interruption of even a short duration. Many other relevant examples can be found in [1-3] and [61].

The cost of poor power quality usually exceeds the cost of measures required for improvement – it is estimated that losses caused by poor power quality cost EU industry and commerce about € 10 billion per annum [63].

Power quality problems have economic impacts on both utilities and customers. Both utility and customer equipment will suffer excessive stress in a poor power quality environment. Power quality disturbances at the utility level may result in the maloperation of remote control, protective devices and energy metering; overheating of cables, transformers and rotating machinery. In the customers' premises, the power quality disturbances may result in the loss of computer data, due to voltage sags, with a duration of only a few milliseconds. Even shorter voltage sags may cause the tripping of industrial drives.

Power quality problems may originate in the system or may be caused by the consumer. The interaction between voltage and current makes it hard to separate the customer as receiving and the network company as supplying a certain level of power

Harmonic currents can cause additional losses and voltage waveform distortions, and so cause poor power quality. Voltage and current harmonics have undesirable effects on power system components and operation. In some instances, interaction between the harmonics and power system parameters (R-L-C) can cause harmonics to amplify with severe consequences. Also, harmonics can lead to improper operation of protective devices, such as relays and fuses. Harmonic currents, particularly of the third order, cause overheating of transformers and neutral conductors. Consumers and distribution systems are sometimes forced to derate their transformers because of the heating effects of harmonic currents. Neutral conductors of supply systems and installations have the same cross-sectional area as phase conductors. There is already evidence of the use of neutral conductors of larger cross-section in newer commercial installations to take account of the increased third harmonic currents. The retrospective installation of such larger neutral conductors in existing networks would result in increased costs, including significant increase in demand for copper and aluminium. Also, the flow of harmonic currents in power supply systems may affect telephone communication. Harmonic voltages in excess of the recommended limits can result in distributors having to replace their transformers, switchgear and lines at prohibitive cost. The resulting networks would be inefficient as harmonic distortion represents reactive power flow.

A DC current can offset the flux excursions in a distribution transformer. As a result the magnetic core of the transformer becomes heavily saturated resulting in excessive heating. Also, the return path for a DC current can often involve current through the earth, sometimes greatly enhancing corrosion of metallic structures (pipes or reinforced steel) buried in the earth.

- *voltage fluctuations* – systematic random or periodic variations in supply voltages;
- *power frequency variations* – deviations of the supply frequency from the nominal frequency (50 Hz or 60 Hz);
- *long duration voltage variations* – r.m.s. variations in the supply voltage at fundamental frequency for periods exceeding one minute. These are classified into *overvoltages*, *undervoltages* and *sustained interruptions*.

2.1.2. Power quality problems and their impacts

The growing number of power electronic-based equipment has produced an important impact on the quality of electric power supply. Both high power industrial loads and domestic loads cause harmonics in the network voltages. At the same time, much of the equipment causing the disturbances is quite sensitive to deviations from the ideal sinusoidal line voltage.

The power quality problems of the major concerns of both customers and utilities are: poor power factor, harmonics in load currents, supply voltage distortion and unbalance, notching in load voltages, DC offset in load currents and voltages, unbalanced loads, voltage sag/swell and flicker [3]. The implications of power quality phenomena and problems are discussed in detail in [1-3] and [61].

Poor power factors are responsible for a substantial increase in the currents flowing in power supply systems and consumer installations, causing a drop in the feeder voltage and increasing the losses.

Understanding power quality issues is a good starting point for solving any power quality problem, and understanding the power quality terms and definitions is basic to getting familiar with the power quality matter. The power quality terminology and definitions are introduced in detail in [61] and [1-3]. A particularly useful overview of power quality terminology with references to standard documents and other valuable sources is given in [2]. Following are the core terms and definitions that are used with power quality:

- *voltage dips (sags)* – reduction of the voltage lasting for half cycle to one minute;
- *voltage swells* – voltage increases lasting for half cycle to one minute;
- *brief interruption* – loss of supply lasting for half cycle to one minute;
- *transients* – voltage disturbances shorter than sags or swells, which are caused by sudden changes in the power systems;
- *voltage notches* – periodic transients occurring within each cycle as a result of the phase-to-phase short circuits caused by the commutation process in a.c.-d.c. converters.
- *voltage unbalance* – a situation, in which either the voltages of a three-phase voltage source are not identical in magnitude, or the phase differences between them are not 120 electrical degrees, or both;
- *waveform distortion* – steady-state deviation in the voltage or current waveform from an ideal sine wave, due to harmonics, which are sinusoidal voltages or currents having frequencies that are whole multiples of the frequency at which the supply system is designed to operate (50 Hz or 60 Hz);

Chapter 2

LITERATURE SURVEY

2.1. Power Quality

2.1.1. Introduction

Power quality is an umbrella term that embraces all aspects associated with amplitude, phase and frequency of the voltage and current waveforms existing in a power circuit. Poor power quality may result either from transient conditions developing in the power circuit or from the installation of non-linear loads. Due to the increasing use of loads sensitive to power quality, e.g. computers, industrial drives, communications and medical equipment, the issue of power quality has gained renewed interest over the last two decades. Nowadays, power quality is an even more complex problem than in the past because the new loads are not only sensitive to power quality but also responsible for affecting adversely the quality of power supply.

Although transmission power systems may have an impact on the quality of power, most power quality problems occur in distribution systems. The power quality becomes significantly worse at the points where the loads are connected to the distribution grid. A single customer may cause significant reductions in power quality for many other customers.

an adaptive dc link voltage controller is proposed for obtaining a better performance of the UPQC both in the steady state and during the transients. The effectiveness of the proposed control strategies is proved through simulations.

Conclusions and future work are presented in **Chapter 7**.

described. It is shown that during the load side short circuit, the series inverter experiences an overvoltage. In order to overcome this problem, a thyristor based protection crowbar is proposed. The principal of operation of the proposed protection circuit is described. Then, its performance is investigated through simulations. Results for four case-studies are presented. The effectiveness of the proposed protection scheme is confirmed through simulation of different fault and system conditions. Also, the experimental results presented at the end of this chapter demonstrate the effectiveness of the proposed protection scheme.

In **Chapter** 5, the UPQC connected to a weak supply point is investigated. The introductory part highlights the problems which appear in cases where the UPQC is connected to a weak supply point. A control approach is proposed for overcoming the stability problem while using the hysteresis band controller. The effectiveness of the proposed control approach is proven both through simulations and experiments. Also, the drawbacks associated with the hysteresis control technique are listed. As an alternative to a hysteresis band controller it is proposed to operate the shunt inverter in voltage control mode, in which case the switching frequency is constant. The appropriate control block is derived and investigated. The effectiveness of this approach is proved through simulations.

Chapter 6 deals with the transient performance of the UPQC. In the introductory part, the problems associated with the load connection/disconnection or supply voltage sag appearance/clearance are explained, based on relevant simulation results. It is shown that during the transient, due to the dc link voltage deviation, the voltage injected by the series converter (and hence the load voltage) can have significant magnitude deviations. For overcoming this problem it is proposed that the amplitude modulation ratio is continuously adjusted to match the actual dc link voltage rather than the reference dc link voltage. Also,

listed and the importance of power quality monitoring is discussed. Solution strategies and mitigation techniques to power quality problems are introduced and an overview of major custom power devices is presented. Network reconfiguring devices are listed, and their basic principle of operation and application are briefly discussed. Then the shunt (Distribution static compensator) and series (Dynamic voltage restorer) active filters are introduced. Finally, the Unified Power Quality Conditioner (UPQC) which integrates the series and shunt active filters is briefly discussed.

Chapter 3 starts with an overview of UPQC power circuit structure and principle of operation. Two possible ways (right- and left-shunt) of connecting the UPQC to the point of common coupling (PCC) are discussed and the advantages of the right-shunt UPQC over the left-shunt are highlighted. The UPQC power circuit design considerations are presented, discussing the selection of three main elements: shunt interface inductor, dc link reference voltage, dc link capacitor. The UPQC control strategy is presented, highlighting the advantages and disadvantages of different control techniques. The following current reference generation techniques are described: average dc voltage regulation, instantaneous p-q theory, synchronous reference frame, discrete Fourier transformations. Also, the hysteresis band current modulation technique (most preferable for shunt active filter applications) is discussed. A UPQC simulation study is performed and simulation results for different case studies are presented. Both UPQC steady state and dynamic performances are investigated. At the end of this chapter the prototype UPQC is described and the experimental results are presented.

In **Chapter 4**, the issues related to UPQC protection against the load side short circuits are investigated. First, the problems involved with a load side short circuit are

3. The UPQC connected to a weak supply point has been investigated and simple to implement control solutions have been proposed for the shunt compensator. A control approach for avoiding the stability problem while using the hysteresis controller has been proposed and its effectiveness has been proved both through simulations and experiments. Also, a control algorithm to operate the shunt inverter in voltage control mode has been proposed. Applying this control approach the switching frequency of the shunt inverter is kept constant. The effectiveness of this control strategy has been proved through simulations.
4. An improved sinusoidal PWM voltage controller for the series compensator has been proposed, which adjusts continuously the control signal magnitude in response to dc link voltage deviations. Also, an adaptive dc link voltage controller has been proposed which diminishes the dc link voltage deviation during the transients and assures negligible steady state error. The effectiveness of the proposed control techniques has been proved through simulations.

1.3. Organisation

This thesis comprises of seven chapters. In **Chapter 2** an overview of power quality issues and solution techniques is presented. First, the power quality terms and definitions are introduced, followed by a summary of power quality problems and their impacts. The importance of power quality is highlighted. Then, the necessity of having power quality standards is explained, and their goals and role in solving power quality problems are presented. The responsibilities of suppliers and users for power quality disturbances are

6. Investigation of UPQC transient performance and development of control techniques for overcoming the problems related to dc link voltage deviations during the transients.

Research has been carried out to achieve the above mentioned objectives and the major contributions of the thesis are:

1. The UPQC general study has been accomplished, comprising of:
   - literature survey;
   - simulation model development and study through simulations;
   - construction and testing of a 12 kVA laboratory prototype (in accordance with responsibilities mentioned above);

   Thus, the effectiveness of the UPQC, in solving the power quality problems has been proved both through simulations and experiments.
2. To protect the UPQC against the load side short circuits a hardware based protection scheme has been derived and its implementation and effectiveness has been investigated. The main protection element is a crowbar consisting of two antiparallel thyristors and connected across the secondary of the series transformer. This protection crowbar is governed by a very simple Zener diode based control circuit. The effectiveness of the proposed protection scheme has been proved both through simulations and experiments. A patent has been filed for this protection scheme. Also, the software based UPQC protection approach has been investigated, the implementation of which does not require additional hardware.

enhancement of power quality in electrical power networks. As part of this project a 12 kVA prototype UPQC has been constructed and tested. The author's responsibilities within this project were:

- building the UPQC simulation model and performing investigations through simulation;
- construction and testing of the prototype UPQC power circuit;
- participation in integration of hardware and software;
- participation in software implementation and debugging;
- participation in final UPQC testing.

The following objectives have been laid down for this research work:

1. Literature survey dealing with: power quality concerns, classic and modern power conditioning solutions;
2. Development of UPQC simulation model and UPQC study through simulation;
3. Construction and testing of the prototype UPQC (in accordance with responsibilities mentioned above);
4. Investigation of UPQC protection issues and development of UPQC protection schemes (both hardware based and digital signal processor (DSP) based control solutions);
5. Investigation of UPQC connected to a weak supply point and development of simple to implement control solutions for shunt compensator;

with both load current and supply voltage imperfections is the Unified Power Quality Conditioner (UPQC) [9], which was first presented in 1995 by Hirofumi Akagi. Such a solution can compensate for different power quality phenomena, such as: sags, swells, voltage imbalance, flicker, harmonics and reactive currents. UPQC is still in the research and development phase, but is very promising. UPQC is a combination of series and shunt active filters connected in cascade via a common dc link capacitor. The series active filter inserts a voltage, which is added at the point of the common coupling (PCC) such that the load end voltage remains unaffected by any voltage disturbance. The main objectives of the shunt active filter are: to compensate for the load reactive power demand and unbalance, to eliminate the harmonics from the supply current, and to regulate the common dc link voltage. In addition, it is preferable that both the series and shunt compensators are operated such that they do not supply or absorb any real power from the ac system during the steady state. A UPQC is an expensive device, as it requires two sets of inverters. However, it is much more flexible than any single inverter based device. Thus, its full capability must be investigated further. Also new applications of this device must be explored to justify its cost.

1.2. Objectives and contributions

This research has been carried out between February 2005 and May 2008 at the School of Electrical Engineering Systems, Dublin Institute of Technology as part of the Unified Power Quality Conditioner (UPQC) research project, supported by Enterprise Ireland. The UPQC research project had as its objective the development of UPQC for the

The fact that power quality has become an issue recently, does not mean that it was not important in the past [1]. Utilities and researchers all over the world have for decades worked on the improvement of what is now known as power quality. There are sets of conventional solutions to the power quality problems, which have existed for a long time. However these conventional solutions use passive elements and do not always respond correctly as the nature of the power system conditions change. The increased power capabilities, ease of control, and reduced costs of modern semiconductor devices have made power electronic converters affordable in a large number of applications. New flexible solutions to many power quality problems have become possible with the aid of these power electronic converters.

Nowadays equipment made with semiconductor devices appears to be as sensitive and polluting as ever [2]. Non-linear devices, such as power electronics converters, increase overall reactive power demanded by the equivalent load, and inject harmonic currents into the distribution grid. It is well known that the reactive power demand causes a drop in the feeder voltage and increases the losses. The presence of harmonic currents can cause additional losses and voltage waveform distortions, and so cause poor power quality. Also, the number of sensitive loads that require ideal sinusoidal supply voltages for their proper operation has increased. The increasing use of electronic equipment sensitive to power variations drives the interest in power conditioning technologies. So, in order to keep the power quality within limits proposed by standards, it is necessary to include some sort of compensation.

The power electronic based power conditioning devices can be effectively utilized to improve the quality of power supplied to customers [3]. One modern solution that deals

Chapter 1

INTRODUCTION

1.1. Power quality concerns

Reliability of supply and power quality (PQ) are two most important facets of any power delivery system today [1]. Not so long ago, the main concern of consumers of electricity was the continuity of supply. However nowadays, consumers want not only continuity of supply, but the quality of power is very important to them too. The power quality problems in distribution power systems are not new, but customer awareness of these problems has recently increased. For example, for many years interruptions shorter than several minutes were not considered as a cause of concern to most consumers. Recently this has changed: more and more equipment is sensitive to very short duration events, and more and more customers (domestic as well as industrial) view short interruptions as a serious imperfection of the supply. In the circumstances when the consumer demands of quality power are rising, the term power quality receives a special significance.

Low quality power affects electricity costumers in many ways [2]. The lack of quality power can cause loss of production, damage of equipment or appliances or can even be detrimental to human health. Therefore, it is very important to maintain a high standard of power quality.

$\hat{V}_{tri}$	Amplitude of the triangular signal
$\hat{V}_{out(1)}$	Magnitude of the fundamental frequency component of the VSI output voltage
V_{dc}	dc link voltage
$V_{dc,act}$	Actual dc link voltage
$V_{dc,ref}$	Reference dc link voltage
$m_{a,ref}$	Amplitude modulation ratio corresponding to the reference dc link voltage $V_{dc,ref}$
$\hat{V}_{out(1),\max}$	Maximum magnitude of the fundamental component of the inverter output voltage in the liner modulation mode
K_p^{50}, K_i^{50}	PI controller parameters corresponding to a LPF with 50 Hz cut-off frequency
K_p^{300}, K_i^{300}	PI controller parameters corresponding to a LPF with 300 Hz cut-off frequency
$V_{dc,av}^{50}$	Average dc link voltage obtained at the output of the LPF with 50 Hz cut-off frequency

v_{a0}, v_{a1}, v_{a2}	Instantaneous symmetrical components for three-phase voltages v_a, v_b and v_c
v_l, v_L	Instantaneous load voltage
v_f	Instantaneous voltage injected by the series active filter
v_t	Instantaneous voltage at the PCC
i_s	Supply current
$i_{s,ref}$	Supply reference current
$i_{f,ref}$	Shunt active filter reference current
$i_s^/$	Not filtered (containing switching harmonics) supply current
$i_{s,ref}^/$	Reference not filtered supply current
C_{sh}	Shunt compensator filtering capacitor
R_{sh}	Shunt compensator damping resistor
$\hat{V}_L$	Load voltage magnitude
$\hat{I}_c$	Magnitude of the fundamental current of the shunt compensator filtering capacitor
$i_L^/$	Instantaneous measured load current after filtering out the noise
$i_{c(1)}$	Instantaneous shunt filtering capacitor fundamental current
$v_{f,ref}$	Shunt inverter reference voltage
m_a	Amplitude modulation ratio
$\hat{V}_{control}$	Magnitude of the control signal

List of symbols

p , q	Instantaneous active and reactive powers
$\overline{p}$, $\overline{q}$	Average active and reactive powers (dc values)
$\widetilde{p}$, $\widetilde{q}$	Ripple active and reactive powers (ac values)
v_α , v_β	Voltages in the α-β frame
i_α , i_β	Currents in the α-β frame
$i^*_{f,\alpha}$, $i^*_{f,\beta}$	Shunt active filter reference currents in the $\alpha - \beta$ reference frame
i_d , i_q	Currents in synchronous reference frame
$\overline{i}_d$, $\overline{i}_q$	dc components (correspond to the fundamental current)
$\widetilde{i}_d$, $\widetilde{i}_q$	ac components (correspond to the harmonic current)
$i_{d,ref}$, $i_{q,ref}$	Shunt active filter reference currents in the synchronous reference frame
$i^*_{f,a}$, $i^*_{f,b}$, $i^*_{f,c}$	Shunt active filter reference currents in *a*-*b*-*c* frame
$\overline{V}_l$	Load voltage in vector form
$\overline{V}_f$	Voltage injected by the series active filter in vector form
$\overline{V}_t$	Voltage at the point of common coupling (PCC) in vector form
i_{a0} , i_{a1} , i_{a2}	Instantaneous symmetrical components for three-phase currents i_a , i_b and i_c

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PQ	–	Power quality
PWM	–	Pulse width modulation
SCR	–	Silicon controlled rectifier
SP	–	Space-vector
SPWM	–	Sinusoidal pulse width modulation
SSB	–	Solid-state breaker
SSCL	–	Solid-state current limiter
SSTS	–	Solid-state transfer switch
SVC	–	Static VAR compensator
THD	–	Total harmonic distortion
UPQC	–	Unified power quality conditioner
UPS	–	Uninterruptible power supply
VSI	–	Voltage source inverter

Abbreviations

CP	–	Custom power
CSI	–	Current source inverter
CT	–	Current transformer or transducer
DFT	–	Discrete Fourier transform
DSP	–	Digital signal processor
DSTATCOM	–	Distribution static compensator
DVR	–	Dynamic voltage restorer
FACTS	–	Flexible ac transmission systems
FFT	–	Fast Fourier transform
GTO	–	Gate turn off thyristor
HPF	–	High pass filter
IEC	–	International Electrotechnical Commission
IEEE	–	Institute of Electrical and Electronics Engineers
IGBT	–	Insulated gate bipolar transistor
LPF	–	Low pass filter
LQR	–	Linear Quadratic Regulator
PCB	–	Printed circuit board
PCC	–	Point of common coupling
PI	–	Proportional integral
PLL	–	Phase lock loop

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I certify that this thesis which I now submit for examination for the award of the Degree of Doctor of Philosophy, is entirely my own work and has not been taken from the work of others save and to the extent that such work has been cited and acknowledged within the text of my work.

This thesis was prepared according to the regulations for postgraduate study by research of the Dublin Institute of Technology and has not been submitted in whole or in part for an award in any other Institute or University.

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Candidate

LC or/and LCL filters are used for interfacing the shunt inverter in order to prevent switching frequency currents entering into the grid. In the presence of such a filter, a hysteresis-controlled shunt inverter fails to follow the reference if it attempts to track the current injected into the grid. A control approach for avoiding the stability problem is proposed with application to the shunt component of the UPQC, incorporating an LCL filter and using the hysteresis controller (which is simple to implement and assures fast response). Also, a control algorithm to operate the shunt inverter in voltage control mode is proposed. Applying this control approach the switching frequency of the shunt inverter is kept constant.

The dc link voltage of the UPQC can significantly deviate from its reference during a transient event, caused by load connection/disconnection or/and supply side voltage sag/swell, though in the steady state, the average dc link voltage is maintained at a certain preset level. Due to dc link voltage deviation, the magnitude of the series injected voltage cannot be constant and this has an effect on the load voltage magnitude, which also fluctuates. An improved sinusoidal pulse width modulation (PWM) voltage controller for the series compensator is proposed, which adjusts continuously the control signal magnitude in response to the dc link voltage deviations. Also, an adaptive dc link voltage controller is proposed which limits the dc link voltage deviation during the transient and assures negligible steady-state error.

Abstract

The proliferation of power electronics-based equipment has produced a significant impact on the quality of electric power supply. Nowadays, much of the equipment is based on power electronic devices, often leading to problems of power quality. At the same time this equipment is typically equipped with microprocessor-based controllers which are quite sensitive to deviations from the ideal sinusoidal line voltage. Conventional power quality mitigation equipment is proving to be inadequate for an increasing number of applications, and this fact has attracted the attention of power engineers to develop dynamic and adjustable solutions to power quality problems. One modern and very promising solution that deals with both load current and supply voltage imperfections is the Unified Power Quality Conditioner (UPQC). This thesis investigates the development of UPQC protection scheme and control algorithms for enhanced performance. This work is carried out on a 12 kVA prototype UPQC.

In order to protect the series inverter of the UPQC from overvoltage and overcurrent during short circuits on the load side of the UPQC, the secondary of the series transformer has to be short-circuited in a reasonably short time (microseconds). A hardware-based UPQC protection scheme against the load side short circuits is derived and its implementation and effectiveness is investigated. The main protection element is a crowbar connected across the secondary of the series transformer and consisting of a pair of antiparallel connected thyristors, which is governed by a very simple Zener diode based control circuit. Also, the software-based UPQC protection approach is investigated, the implementation of which does not require additional hardware.

DEDICATED TO MY PARENTS

WIFE

AND CHILDREN

UNIFIED POWER QUALITY CONDITIONER:
Protection and Performance Enhancement

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A thesis submitted for the Degree of Doctor of Philosophy
to the Dublin Institute of Technology

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